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Operating and Service Manual

OS3500
60MHz DUAL TRACE OSCILLOSCOPE

a/so → 053600

MP MASTER
MA34658

GOULD
An Electrical/Electronics Company

GOULD

Manual Part No.
80-OS3500

OS3500
60MHz DUAL TRACE OSCILLOSCOPE

a/so → O 53600

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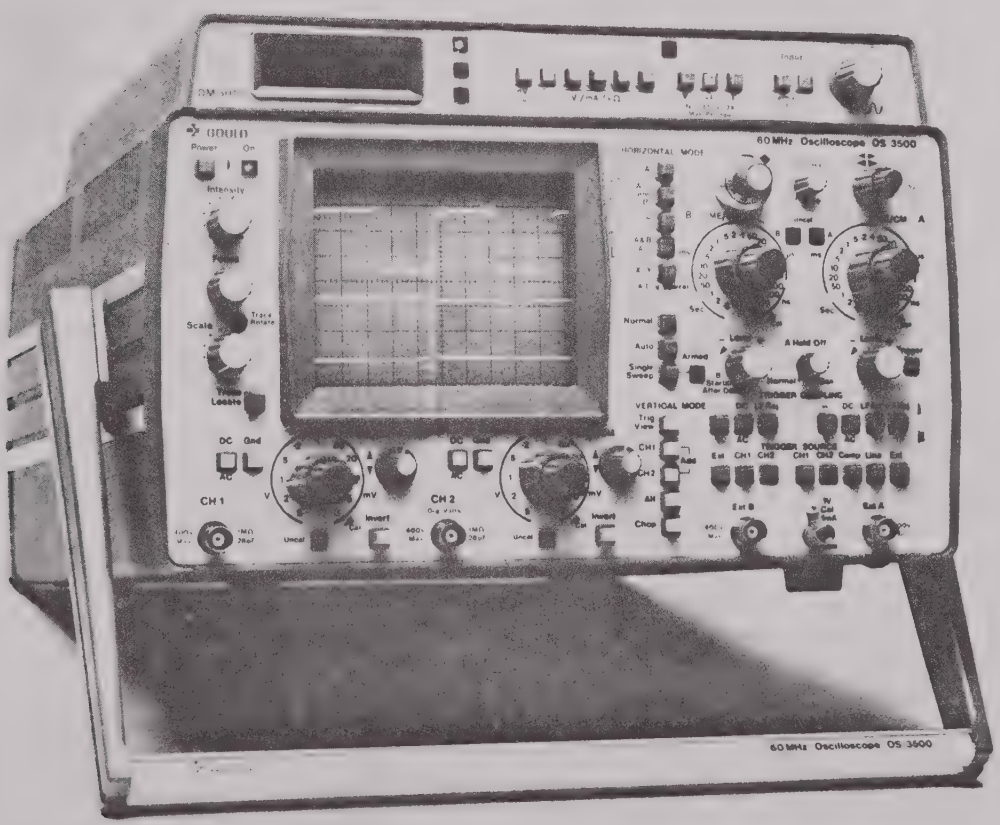
Introduction

Section 1

The Gould OS3500 is a general purpose 60MHz dual trace oscilloscope. Its high sensitivity and fast sweep speed make it suitable for a wide range of laboratory or production applications in both the analog and digital fields.

It has a full dual timebase with comprehensive independent triggering facilities for each. These, with a variable hold-off capability, make it particularly suitable for the examination of complex waveforms. The display modes include alternate A and B timebase sweeps and a trigger view facility allows the external or internal trigger input signal to be displayed as a third trace on the screen. The bright 8 x 10cm display with illuminated internal graticule allows the display of fast transients.

The front panel controls are grouped for ease of operation and the construction and weight make it a readily portable instrument. The Digital Measurement option extends the capabilities of the instrument to provide direct digital readout of voltage, time or equivalent frequency from the oscilloscope and it can operate independently as a digital multimeter.



Specification

Section 2

DISPLAY

CRT	8 x 10cm rectangular
EHT	12kV overall
Graticule	Internal, with 8 x 10cm divisions and 2mm sub-divisions. Continuously variable illumination.
Phosphor	P31 standard, P7 option.
Beam Finder	Compresses trace to within graticule area regardless of settings of the vertical and horizontal position controls. Provides pre-set brilliance level.

VERTICAL DEFLECTION

Input Channels	Two identical
Bandwidth	DC-60MHz (−3dB), DC coupled 2Hz-60MHz (−3dB), AC coupled
Rise Time	<6ns
Input Coupling	DC – Ground – AC
Input Impedance	1MΩ/28pF
Deflection Coefficient	2mV/cm to 5V/cm in 11 ranges (1-2-5 sequence) with uncalibrated fine gain control giving a 2.5:1 reduction in gain. Warning light indicates uncalibrated condition.
Accuracy	±3%
Position Control	Shift range ±8cm
Signal Delay	At least 0.5cm (25ns) of visible delay
Max. Input Voltage	400V (DC plus AC pk.)
Display Modes	CH1 only CH2 only CH1 and CH2 chopped (500 kHz approx). CH1 and CH2 alternate CH1 and CH2 added Trigger View Trigger View, CH1 and CH2 alternate Trigger View alternate with CH1 and CH2 chopped N.B. Channels 1 and 2 can be inverted
Trigger View	Enables the main timebase trigger signal to be continuously displayed. A trigger signal derived from an external source will have a deflection coefficient of approximately 100mV/cm

HORIZONTAL DEFLECTION

Display Modes	Main Timebase Main Timebase intensified by Delayed Timebase Delayed Timebase Main and Delayed Timebase simultaneously (alternate sweeps) X-Y, with CH1 or CH2 providing X-deflection input X-Y_1/Y_2 with line or ext. trig. socket providing X-deflection input

	Main Timebase (A)	**Delayed Timebase (B)**
Sweep Speeds	50ns/cm to 0.5s/cm in 22 steps (1-2-5 sequence)	50ns/cm to 0.5s/cm in 22 steps (1-2-5 sequence)
Fine Sweep Control	Uncalibrated. Reduces sweep rate by at least 2.5 times (longest sweep approx. 12.5s). Warning light indicates uncalibrated condition.	Uncalibrated. Reduces sweep rate by at least 2.5 times (longest sweep approx. 12.5s). Warning light indicates uncalibrated condition.
Expansion	X10, gives max. sweep rate of 5ns/cm.	X10, gives max. sweep rate of 5ns/cm.
Accuracy	±3% (±5% with X10 expansion).	±3% (±5% with X10 expansion).
Sweep Delay	A 10-turn calibrated vernier control operates with reference to the main timebase setting. Control of delayed timebase start variable from 0.2cm to 10.2cm. Differential Accuracy: ±1.5% rdg. ±0.1% f.s. Jitter: <1 in 10000 of full scale.	The delayed timebase can be started at the end of delay or triggered after the delay.

Trace Separation	Operates in A and B timebase alternate sweep mode and provides ±3.0cm min. Y shift on the B sweep.

	Trigger (A)	**Trigger (B)**
Source	Internal CH1	Internal CH1
	Internal CH2	Internal CH2
	Composite (CH1/CH2)	External
	External	
	Line	
Slope	Pos/Neg	Pos/Neg
Coupling	DC, AC, AC(LF rej.), DC(HF rej.)	DC, AC, AC(LF rej.)
Modes	Manual level	Manual level
	Auto (bright-line)	Start after delay
	Single sweep	

	Trigger (A)	Trigger (B)
Sensitivity	Internal: To 10MHz ⩽2mm (Below 50Hz sensitivity decreases when AC coupled) 10MHz-100MHz ⩽1cm	Internal: to 10MHz ⩽2mm (Below 50Hz sensitivity decreases when AC coupled) 10MHz-100MHz ⩽1cm
	External: To 10MHz ⩽40mV	External: To 10MHz ⩽40mV
	(Below 50Hz sensitivity decreased when AC coupled) 10MHz-100MHz ⩽200mV	(Below 50Hz sensitivity decreases when AC coupled) 10MHz-100MHz ⩽200mV
	Level range (internal): ±8cm approx.	Level range (internal): ±8cm approx.
	Level range (external): ±1.6V approx.	Level range (external): ±1.6V approx.
External Trigger	Input impedance 1MΩ/28pF Max. input voltage 400V (DC plus AC pk.)	Input impedance 1MΩ/28pF Max. input voltage 400V (DC plus AC pk.)
Trigger Hold-off	Continuously variable up to approx. one sweep length of main timebase, except for three slowest ranges.	

HORIZONTAL AMPLIFIER

Bandwidth	DC – 1.5MHz (–3dB)
Deflection Coefficient	200mV/cm
Accuracy	±15%
Input Impedance	1MΩ/28pF
Max. Input Voltage	400V (DC + AC pk.)
X-Y Operation	With X input via External Trig. socket, X specification as above. With X input via CH1 or CH2, sensitivity as attenuator setting but accuracy ±15% (CH1) or ±5% (CH2). Phase error <3° at 500kHz.

CALIBRATOR

Voltage	1V ± 1%
Frequency	1kHz approx.

Z-MODULATION

Bandwidth	DC to 10MHz
Sensitivity	+4V from zero gives complete blanking
Input Impedance	2.2kΩ

OUTPUTS

Main Timebase Ramp	Output level zero to +4V from source impedance of 10kΩ
Delayed Timebase Gate	Output level +3V to zero from source impedance of 10kΩ

SUPPLIES

Voltage	100V; 120V; 220V; 240V ±10%
Frequency	45 – 440Hz
Consumption	80VA

TEMPERATURE RANGE

Operating	0 to 50°C
Operating within spec.	+15°C to +35°C

SIZE AND WEIGHT

Size	32.5cm x 18.0cm x 46.5cm (w x h x d) exc. handles and knobs.
Weight	10kg (22 lb)

ACCESSORIES SUPPLIED

2 off 80MHz probe kits with x10 and x1 switched heads, PB12.
1 off Supply Lead PL98.

OPTIONAL ACCESSORIES

Viewing Hood, PN42224
Protective Cover (soft), PN42225
Front Panel Cover (hard), PN42226
Trolleys, TR4 or TR6
Rack Mount Kit, PN42227
250MHz x10 Probe Kit PB14
100MHz x100 Probe Kit PB15

ADD-ON DIGITAL MEASURING UNIT DM3010

The optional unit, DM3010, provides a 3½ digit DVM facility, via a separate floating input and increased voltage and time accuracies when switched to operate with the OS3500. The DM3010 can be supplied already fitted to the oscilloscope or retro-fitted by a Gould approved service centre.

When used with the OS3500 in the measurement of amplitude, time and frequency the following accuracies are achieved:-

Amplitude:	±2.0% ± 2 digits
Time:	±1.0% ± 2 digits
Frequency:	Accuracy calculated from reciprocal of equivalent period ± 1 digit.

Amplitude accuracy is condtioned above 5MHz by the vertical amplifier roll-off to −3dB at 60MHz.

DC voltage measurements, in the DVM mode, can be made in the range 200mV f.s. to 1000V f.s. with a maximum resolution of 100μV and accuracy of ±0.15% r.d.g. ± 1 digit in the 200mV range. Accuracy of other DC voltage ranges is ±0.1% r.d g. ± 1 digit. Resistance can be measured from 200Ω f.s. to 2MΩ f.s. at an accuracy of ±1.0% r d g ± 1 digit and Current from 200μA f.s. to 2A f.s. at an accuracy of ±0.2% r.d.g. ±1 digit.

3.1 SWITCHING ON

CAUTION. The OS3500 is convection cooled and must always be operated in a position such that air circulating through the bottom and side vents is not restricted.

1. Set the support/carrying handle to the required operating position. The handle is released by pulling outward both fixing bushes when it can be turned to lock in any of 5 positions.
2. Before connecting the OS3500 to the supply, check that the supply range switches are set to suit the supply voltage to be used and that the correct fuse is fitted. Note that the fuse has to be changed when switching between the 100V and 220V ranges. The switches and fuse holder are mounted on the back panel of the instrument. Do not operate the range selection switches while the OS3500 is switched on.

SAFETY: The OS3500 is designed to be used with the frame grounded and it is important that the appropriate lead (Green/Yellow) of the supply lead, PL98, is connected to a suitable ground.

3. Push the POWER button and ensure that the indicator lamp lights. A trace should be obtained with 1 minute and full calibrated performance within 15 minutes.

3.2 OBTAINING A TRACE

1. To obtain a trace:
   a. Select CH1 on VERTICAL MODE switch.
   b. Select A on HORIZONTAL MODE switch.
   c. Select AUTO on NORMAL/AUTO/SINGLE sweep switch.
   d. Operate TRACE LOCATE button, adjust horizontal shift and CH1 shift to centralise the horizontal trace. These controls are identified by the horizontal and vertical arrows.
   e. Release TRACE LOCATE and adjust INTENSITY and FOCUS to obtain a sharply defined trace of reasonable intensity.

      If the TRACE LOCATE is operated at any time a trace will appear on the screen if the timebase is running, A spot will appear if the timebase is not triggered or X-Y has been selected as the Horizontal Mode.

   f. If necessary, adjust TRACE ROTATION for precise alignment of trace with the center graticule line.

3.3 SETTING OF A Y CHANNEL

1. Using a coaxial lead (PL43) or suitable probe, connect a signal to CH1 input socket.
2. a. For direct coupling of the input signal select DC on the input coupling switch.
   b. For coupling via the internal 0.1μF capacitor select AC.
3. a. Adjust the VOLTS/cm switch and vertical shift to obtain the required vertical deflection.
   b. If necessary adjust the concentric VARIABLE control away from its calibrated clockwise position. A warning UNCAL light is lit when this is done.
4. To locate the ground or zero volt level select GND on the input coupling switch. This open circuits the input signal and grounds the amplifier input.
5. If under this GND condition a vertical trace movement is observed on adjustment of the VOLTS/cm switch, reset the STEP BAL preset control for that channel. Access to this is through the bottom cover. This should not be done within 15 minutes of switching on.
6. Deflection which is normally positive-up may be inverted by selecting INVERT.

3.4 DUAL CHANNEL OPERATION

1. Signals applied to CH2 and CH2 inputs can be displayed simultaneously by selecting ALT on the vertical mode switch on timebase ranges faster than about 1ms/cm and CHOP at slower sweep speeds.
2. Signals applied to CH1 and CH2 may be added to or subtracted from each other by selecting ADD on the vertical mode switch and if required operating the invert switches on either channel.

3.5 TRIGGER VIEW OPERATION

Whatever vertical mode has been selected, pushing the TRIG VIEW button on the vertical mode switch -bank will bring up another trace showing the signal in the A trigger amplifier. This applies to any trigger source except COMPOSITE, thereby giving three channel operation when the External Trigger source is selected. This facility is covered fully in section 3.8.

3.6 A TIMEBASE OPERATION

The speed of the A timebase is determined by the setting of the A TIME/cm switch. A variable TIME/cm control is fitted concentrically with the A TIME/cm switch which provides a further 3:1 (approx.) variation. When the variable control is turned in an counterclockwise direction from its switched CAL position a red warning light illuminates to show that the A timebase is no longer calibrated.

The gain of the internal X amplifier may be increased by ten times by pulling out the PULL X10 control on the inner shift control. This facility is available at all settings of the timebase but not when the X-Y mode is selected. The facility effectively increases the sweep length from 10cm to 100cm and thus allows close examination of any portion of the trace. Any portion of the increased sweep length may be selected for viewing on the display by adjusting the X shift controls (identified by horizontal arrows). The fine shift control will move the display by approximately 1cm when X10 is not selected and by 10cm in the magnified mode.

A particular advantage of this facility is to increase the maximum sweep speed to 5ns/cm.

1. To adjust the time scale of the horizontal axis:
   a. Set the A TIME/cm switch to the required setting.
   b. If necessary, adjust the concentric VARIABLE.

3.7 A TRIGGER

The A timebase may be triggered by the following sources as selected from the 5-way push button bank.

a. CH1 or CH2 selects the output of the appropriate amplifier (irrespective of which beam is displayed).
b. COMP (Composite) selects a mixture of CH1 and CH2 signals such that each channel may produce a stable trace (see note at the end of this section).
c. LINE The power supply line input frequency derived internally from the supply transformer.
d. EXT An external triggering source connected to the EXT A socket.

The A LEVEL control allows selection of the triggering point on the trigger waveform and hence determination of the start of the horizontal trace.

The A Trigger Coupling push button switches are used in conjunction with the Trigger Source switches to connect different networks into the trigger amplifier circuit, and are effective for all settings of the Trigger Source switches.

The four switch positions for the A Trigger Coupling are able to latch independently; the functions are detailed as follows:

1. Positive/Negative (marked +/–) determines whether trigger occurs as the input signal passes the selected trigger level in a positive or negative-going direction. This allows the amplifier to trigger on positive-going leading edges when positive is selected (button in out position) or negative-going leading edges with the button pressed in. + is with the button out and – with it in.
2. DC/AC. The ac (button out position) is useful for wideband trigger on most signals. The dc position is also a wideband trigger mode but is most useful at very low frequencies or when the mark-space ratio of a pulse signal is likely to vary. The Y input coupling must also be set to DC for this mode to be effective on internal trigger.
3. LF REJECT. A filter is switched into circuit to reject low frequencies. High frequency triggering may be effected from complex waveforms containing high frequency components. Note that this switch position automatically reverts the trigger amplifier to an ac coupled mode even if dc trigger has been selected.
4. HF REJECT. A dc coupled filter is switched into circuit to reject high frequencies. Low frequency triggering may be effected from complex waveforms containing high frequency components.

Note 1
Since the composite trigger signal is taken after the beam switch, its use is relevant only on dual trace displays in the ALT (alternate CH1 and CH2) mode. Reliable triggering is obtained only with dc trigger coupling when the two traces overlap. In this mode the level control defines a point on the display rather than a level of input signal and the trigger point on the waveforms is altered with the Y shift controls.

The main application of this trigger mode is to display two signals of unrelated frequency. Relative phase relationship is lost when displaying signals of the same or related frequency.

Triggering control is effected as follows:

1. Select an A Trigger Source push button for the required trigger signal.
2. Set the timebase to display A sweep.
3. Set the A Trigger coupling for the desired trigger input requirements.
4. Adjust the LEVEL control so that the trace starts at the required point on the waveform. The Trigger View position may be used as a guide to trigger level to assist with this setting procedure (see next section).

3.8 TRIGGER VIEW

This switch is grouped with the Vertical Mode Y channel switches. It may be latched independently and provides an extra trace for viewing the trigger signal as it passes through the A trigger amplifier. The trigger view signal may be viewed together with one or both of the Y signals so selected, alternatively it may be viewed on its own if the other Vertical mode switches are all out.

Trigger view is not available when Composite trigger or A and B ALT is selected.

The Trigger view trace has three main functions.

a. It gives a guide to trigger level. The center horizontal line of the graticule corresponds approximately to the dc level of the waveform that the trigger amplifier will select.
b. It enables the effectiveness of the LF Rej. and HF Reg. to be observed when filtering is required on a particular signal.
c. It enables a third Y channel to be available via the EXT A input socket when the EXT Trigger Source is selected. The trigger view trace must, however, be central on the screen for the instrument to be triggered in this mode.

Note 1.
When viewing signals from CH1 or CH2 the sensitivity of the Trigger view display is approximately double that which is selected on the Y channel attenuator switches. The sensitivity to external trigger signal is approximately 100mV/cm. Bandwidth of this trace may be only half that of the two Y channels.

Note 2.
If a timebase speed slower than 1ms/cm is selected, then flicker may be observed when using the trigger view as this function operates only in an alternate mode.

3.9 TRIGGER MODES (Normal, Auto & Single Sweep)

These are selected on the 3-way interlocking push button bank mounted above the Y channel switches.

3.9.1 NORMAL

This mode is relevant for all trigger signals from d.c. to h.f. The trace will blank in absence of trigger signal.

3.9.2 AUTO

In the absence of a trigger signal this provides a bright-line, so that the existance of any signals present may be observed (although not necessarily triggered). When the timebase is triggered the bright-line function is switched out automatically, and a normal trigger state exists.

AUTO is useful for wideband signals above 40Hz. Operation below this frequency may cause mis-triggering since the timebase can revert periodically to its bright-line state.

3.9.3 SINGLE SWEEP

This facility is useful for observing a single event, particularly if a photographic record is required. By pressing the SINGLE SWEEP push button the NORMAL and AUTO buttons will be in the out position and the 'ARMED' l.e.d. indicator will illuminate showing that the timebase is ready to be triggered. On receipt of a trigger signal the timebase will operate and provide one single sweep only. To initiate further sweeps it is necessary to re-arm the timebase by pushing the single sweep button again. The single sweep facility is switched out when NORMAL or AUTO are selected again. The procedure for operating the timebase to give a single sweep is as follows:-

1. Apply a repetitive waveform and obtain a trace with the sweep switch in the NORMAL mode by adjusting the A LEVEL control.
2. Press SINGLE SWEEP button and triggering should then cease. The ARMED indicator should then illuminate in readiness for the trigger signal.
3. The next trigger pulse will initiate a sweep and the l.e.d. indicator will be extinguished on completion of the sweep. The timebase will not operate again until the SINGLE SWEEP button is pressed again.

3.10 A HOLD OFF

When the A HOLD OFF control is in its normal position, switched fully counterclockwise, the hold-off circuit provides sufficient delay for the timebase to recover before the start of the next sweep. When used as a variable control its main function is to provide simpler triggering on complex waveforms. In most positions of the timebase range switch the range of hold-off variation is about equivalent to the time taken for the timebase to complete one sweep. In the case where the timebase is required to be triggered on a complex waveform (e.g. a repetitive logic pulse pattern containing pulses of different widths) then the hold-off may be used to inhibit trigger until the desired period in the waveform is reached.

To trigger on complex waveforms.

1. Adjust the A TIME/cm switch such that the repetition time of the waveform pattern is within the total time of the timebase sweep. Adjust the trigger control in the normal manner until the Trigger indicator lights.
2. Adjust the HOLD-OFF control for a stable trace.

NOTE: When triggering at high frequency if any small jitter is visible on the trace, this may be removed by fine adjustment of the HOLD-OFF control.

3.11 B TIMEBASE AND TRIGGER

The speed of the B timebase is determined by the B TIME/cm switch which has all the ranges of the A TIME/cm switch. The B TRIGGER SOURCE selection is similar to that for the A channel but does not incorporate LINE or COMP trigger. The B TRIGGER COUPLING is also similar to the A channel but without the HF Reject push button. The B trigger level control operates in a similar manner to the A LEVEL control but incorporates the B STARTS AFTER DELAY switched position at its extreme counterclockwise position.

3.12 DUAL TIMEBASE OPERATION – NORMAL DELAYED SWEEP

To examine a small period of a stable 'A' sweep:

1. Set the B TIME/cm about two ranges faster in speed than the A TIME/cm switch.
2. Rotate the B LEVEL control fully counterclockwise to the switch position, B STARTS AFTER DELAY.
3. Set the HORIZONTAL MODE switch to A INTENS by B.
4. Adjust the INTENSITY control to observe the intensified part of the trace.
5. Adjust the B TIME/cm and the delay multiplier potentiometer so that the intensified portion covers the period of interest.
6. Move the HORIZONTAL MODE switch to the B position when the intensified section of the previous trace will be expanded to form the full trace. Make final adjustments to the DELAY control and B TIME/cm switch to examine the point of interest as required.

3.13 DUAL TIMEBASE OPERATION – GATED SWEEP

If the display exhibits annoying jitter because of a high degree of expansion or unstable trigger of the A sweep:

1. Return to the A INTENS BY B display position.
2. Select the appropriate trigger source slope and coupling on the B push button switches.

3. With the B LEVEL still in the B STARTS AFTER DELAY position adjust the DELAY control so that the bright-up starts just before the edge of the waveform selected as A trigger points.
4. Rotate the B LEVEL control clockwise and adjust for a stable trigger by observing the bright-up.
5. Select 'B' on the HORIZONTAL MODE switch.

3.14 DUAL TIMEBASE OPERATION – A & B ALTERNATE SWEEPS

This allows the A sweep and delayed B sweep to be observed on alternating timebase cycles. The traces may be prevented from overlapping by use of the TRACE SEPARATION control which provides up to about ±4cm of additionally shift to the B trace only. When CH1 and CH2 are displayed in the ALT mode the trace sequence displays 2 A sweeps (CH1 and CH2) and then 2 B sweeps (CH1 and CH2).

To display A and B ALT proceed as follows:

1. Set the HORIZONTAL MODE to display A only and obtain a display using only the 'A' timebase controls.
2. Set the B TIME/cm switch two ranges faster in speed than the A TIME/cm switch.
3. Set the B LEVEL to B STARTS AFTER DELAY.
4. Press the A and B ALT switch and adjust the TRACE SEPARATION control to move the traces a reasonable distance apart. Then finally adjust the DELAY control and B TIME/cm for best display.

3.15 EXTERNAL X

In this condition the timebase is switched off and the external signal is applied directly to the internal X amplifier to produce a horizontal deflection (180mV/cm approx.). Dual trace Y operation may be used if CHOP is selected.

1. Set the HORIZONTAL MODE switch to X-Y.
2. Set the A TRIGGER SOURCE switch to EXT and TRIGGER COUPLING to dc without LF or HF Reject
3. Apply the X signal via the EXT A socket.

For both EXT X and X-Y operation the Trigger coupling networks are still functional, i.e. it is possible to introduce ac coupling or either of the rejection filters into the X deflection path. The +/– invert function, however, is not available.

3.16 X-Y MODE

It is possible to use the flexibility of the two Y inputs for X-Y displays.

1. Set the HORIZONTAL MODE switch to X-Y.
2. Set the TRIGGER SOURCE switch to CH1 or CH2, depending on which channel is desired for the X display. The TRIGGER COUPLING switch should be set to dc, without selection of LF or HF Reject.
3. Select the appropriate channel on the VERTICAL MODE switch for the Y display.

The sensitivities on X-Y will be as the calibrated Y attenuator switches. Note that the accuracy in better in the X direction if the CH2 display is used to display X and CH1 for Y.

3.17 Y-LINE MODE

By using the instrument in the X-Y mode and pressing the LINE TRIGGER SOURCE switch, a display of Y versus supply line frequency may be obtained.

3.18 ADDITIONAL FACILITIES

3.18.1 USE OF PASSIVE PROBE

An X10 passive probe may be used to extend the voltage range and increase the input impedance of the Y amplifiers. The input impedance of the instrument is 1MΩ shunted by 28pF. The effective capacity of the input lead must be added to this and the resultant impedance will sometimes load the signal source. The probe will reduce this to approximately 10pF and increase the resistance to 10MΩ. To obtain a flat frequency response it is necessary to adjust the probe capacitance to match capacitance of the oscilloscope as follows:

1. Set the VOLTS/cm switch to 20mV/cm, and the A TIME/cm switch to 0.2ms/cm.
2. Connect the probe to the 1V CAL pin.
3. Set the adjustable capacitor in the probe tip or termination, with a small screwdriver, for a square response with no overshoot or undershoot.

3.18.2 1 VOLT CAL OUTPUT

This pin provides a positive-going square wave of 1V ± 1% at approximately 1kHz. Shorting this pin to ground will give a square current waveform of 1mA in the shorting link, for current probe calibration.

3.18.3 REAR PANEL OUTPUTS

Two BNC sockets on the rear provide:

1. A ramp, a 4V positive-going sawtooth waveform, from a 10kΩ source impedance.
2. B gate, an approximately +3V level going to ground for the duration of the B sweep.

3.18.4 Z MODULATION

This 4mm socket allows dc coupled blanking to be applied to the c.r.t. The c.r.t. trace is blanked by a positive input. Negative inputs have no effect. The required amplitudes are:

a. +1V for visible modulation

b. +4V for blanking at *normal* intensity

The input impedance is approximately 2kΩ.

4.1 SYSTEM DESCRIPTION

The block diagram for the instrument is shown in Fig. 1. It is not intended to be a full logic diagram but details the functional points of the circuit and their inter-relation. The circuit can readily be divided into two main sections which are the Y and X deflection circuits, the latter includes the two timebases with their associated trigger systems.

4.1.1 Y CHANNELS

The switched Attenuator, Preamplifier and Trigger Amplifiers are identical for the two Y channels. CH2 differs in having external DVM shift facilities. The state of the decade steps of attenuation and amplifier gain switching are determined by the sensitivity selected.

The Beam Switch is a fast electronic switch with the equivalent of a changeover action. It selects either the CH1 or the CH2 signal to be passed to the subsequent stages and is controlled from a bistable. In the chop mode the bistable is driven by continuous pulses from the free running oscillator, switching the beam between the CH1 and CH2 signals as the X sweep progresses. In the alternate mode, the bistable is reversed at the end of each timebase sweep, giving alternate CH1 and CH2 sweeps.

When Trigger View only is selected, the Trigger View Channel Switch selects the chosen A Trigger signal as the Y deflection signal instead of the CH1 and/or CH2 signals. When this function is selected with CH1 and/or CH2, Trigger View Bistable operates on an alternate sweep manner to provide the required two or three trace display.

The signal from the selected channel is passed via a delay line and amplifiers to the Y deflection plates of the c.r.t. This delay allows examination of that point in the waveform which initiated the sweep because the deflecting signal reaches the Y plates after the time-base sweep has been initiated and the trace brightened.

4.1.2 A TIMEBASE OPERATION

The purpose of the timebase system is to generate a linear ramp or ramps to deflect the spot in the X direction. The trigger system initiates each sweep from the incoming or other signals, normally to obtain a stationary display of a repeated waveform. Two timebase systems are included to allow detailed examination of a chosen section of a waveform. The A Timebase is used for simple sweeps described above and the B Timebase is introduced to provide the expansion when required.

The internal or external signal as selected is amplified by the Trigger Amplifier to drive a trigger circuit. If the timebase is ready to commence a sweep, a transition of the trigger circuit will set the 'A' Time-base bistable which in turn initiates the 'A' ramp. This signal is passed through the Sweep Select switch and X Output Amplifier to the X deflection plates of the c.r.t.

At the end of the sweep, when the ramp reaches the required level the bistable is reset, returning the ramp to its original level. During the recovery period the bistable is held reset and this inhibition is maintained by the Hold Off circuit until the ramp generator is fully recovered, ready for the next sweep to commence on the next trigger pulse, when the cycle repeats.

The Bright Up Amplifier normally holds the c.r.t. beam in the cut-off state. The output of the 'A' Bistable which allows the 'A' ramp to operate, also feeds the Bright up Amplifier to raise the intensity of the c.r.t. spot to the level determined by the intensity control.

At the end of the sweep, this output of the bistable is reset and blanks the trace during the flyback period.

If the Y channels are being switched in the chopped mode, the output of this multivibrator is also fed to the Bright Up Amplifier to blank the trace while the Y switching transition takes place. This leaves the appearance of two separate traces for CH1 and CH2 on the screen unless the sweep speed is higher than that normally recommended for chop operation.

4.1.3 TRIGGER MODES

The trigger signal for either timebase, selected from either channel internal, external or line frequency sources, is a.c. or d.c. coupled before being fed into the trigger amplifier which is biased by the required trigger level and the resultant output passed to the trigger circuit to be squared up be the Schmitt trigger.

In the Auto mode, the A Timebase is made to free run in the absence of a trigger signal so giving a bright line reference when, for example, the Y inputs are grounded.

In Single Sweep, the Single Shot bistable normally inhibits trigger pulses from reaching the 'A' timebase bistable. When the bistable is set manually, the next trigger pulse initiates one sweep and the Single Shot bistable is reset, preventing the timebase from sweeping again.

4.1.4 X EXPANSION

The gain of the X Output Amplifier normally allows the ramp to deflect the spot slightly more than the full 10cm of X scan. The X10 X Expansion increases this gain accordingly giving a full sweep display of greater than 100cm and the X Shift control determines which 10cm portion of this appears on the screen. This facility is available on all timebase modes of display, but not on XY.

4.1.5 B TIMEBASE OPERATION

'A' INTENSIFIED BY 'B' ('B' STARTS AFTER DELAY)

In this mode of operation the 'A' ramp is the same as for 'A' only. The 'B' timebase bistable is switched on at the required point in the 'A' sweep when the 'A' ramp reaches the potential set by the delay control and detected by the Delay Comparator. The 'B' ramp

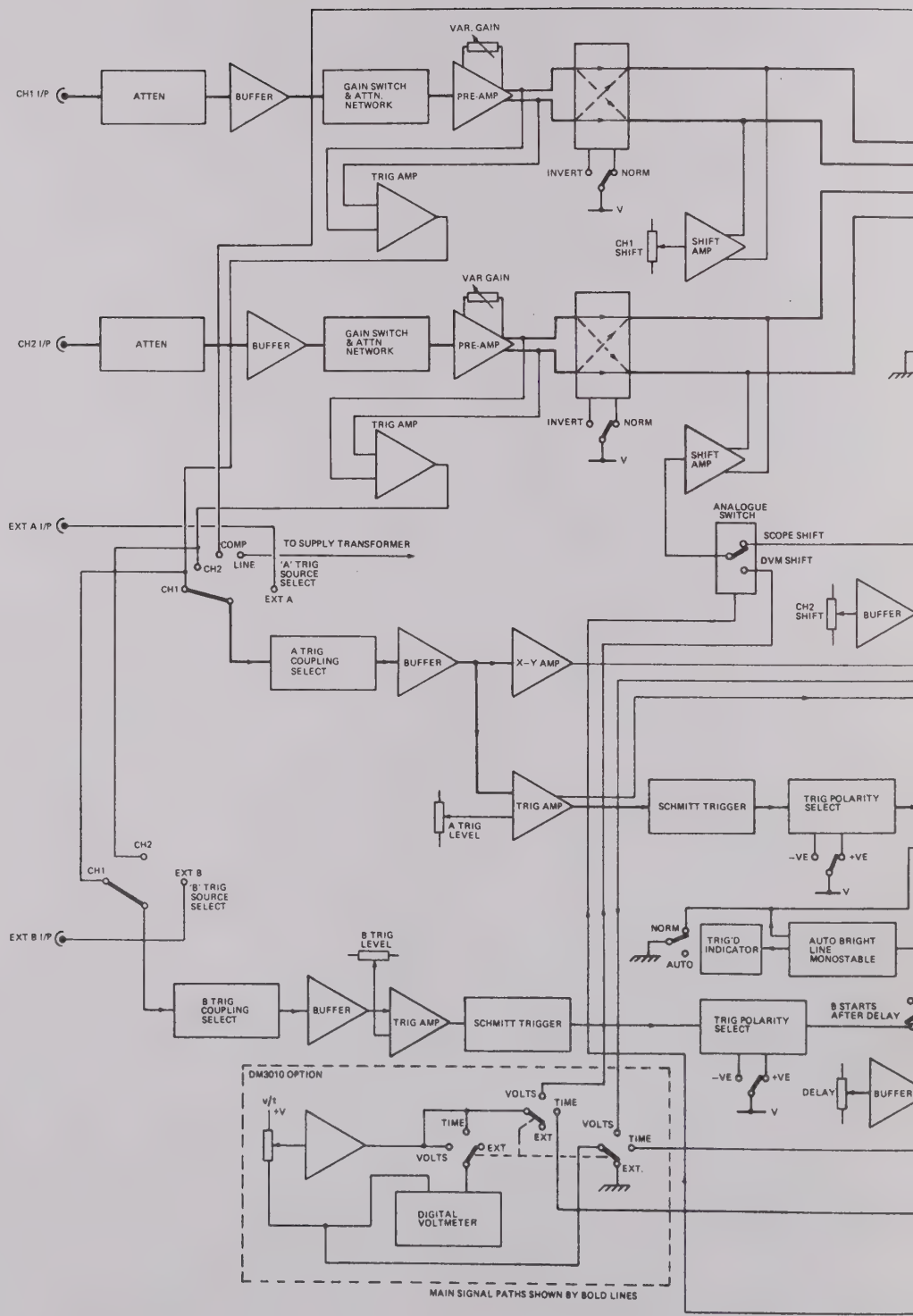
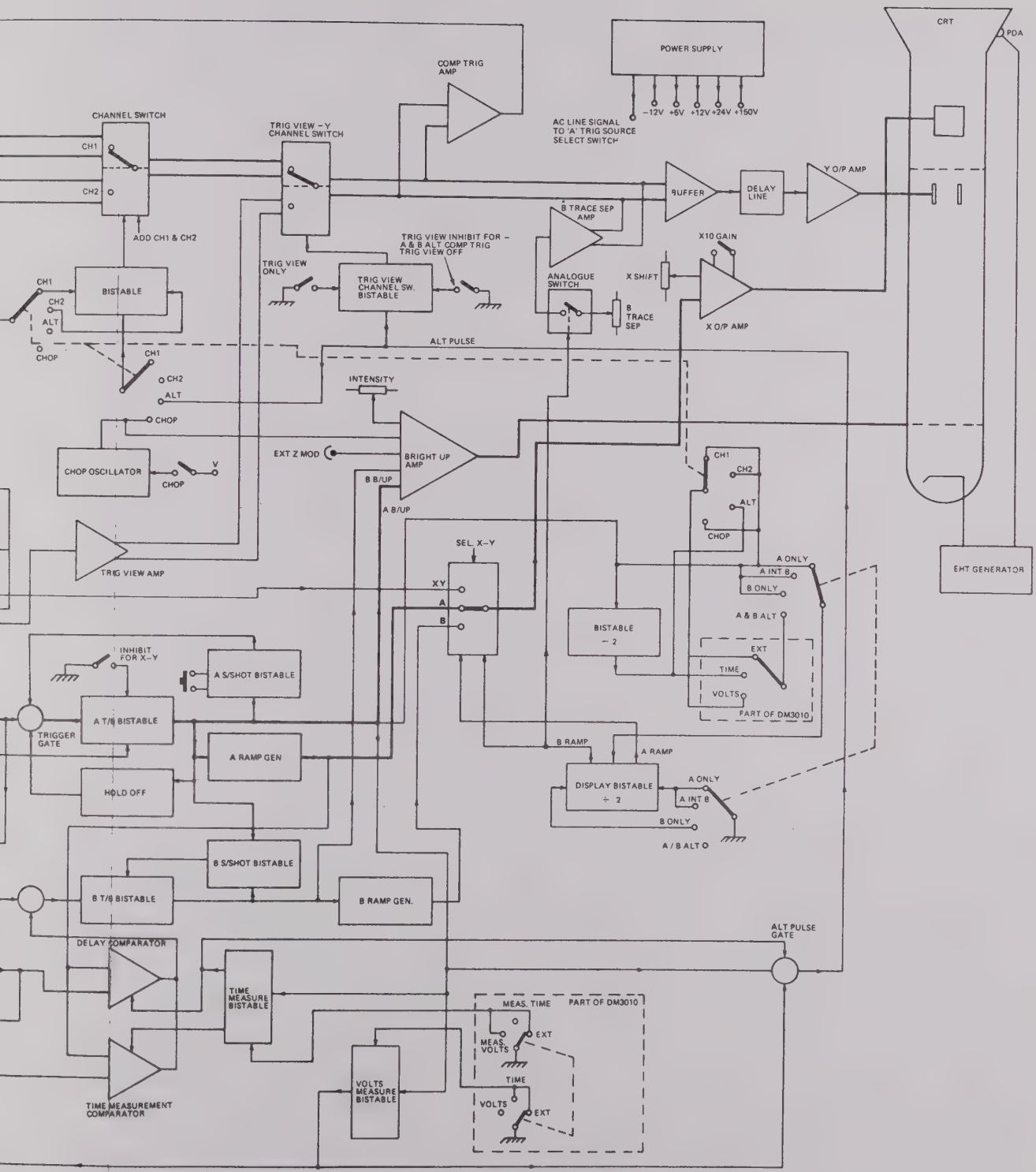


Fig. 1 Block Diagram


CRT
PDA
POWER SUPPLY
−12V +6V +12V +24V +150V
AC LINE SIGNAL TO 'A' TRIG SOURCE SELECT SWITCH
COMP TRIG AMP
CHANNEL SWITCH
CH1
CH2
TRIG VIEW – Y CHANNEL SWITCH
BUFFER
DELAY LINE
Y O/P AMP
B TRACE SEP AMP
ADD CH1 & CH2
TRIG VIEW INHIBIT FOR – A & B ALT COMP TRIG TRIG VIEW OFF
TRIG VIEW ONLY
TRIG VIEW CHANNEL SW. BISTABLE
X10 GAIN
ANALOGUE SWITCH
X SHIFT
B TRACE SEP
X O/P AMP
BISTABLE
ALT
CHOP
ALT PULSE
INTENSITY
EXT Z MOD
BRIGHT UP AMP
B B/UP
A B/UP
CHOP OSCILLATOR
V
TRIG VIEW AMP
SEL. X–Y
XY
A
B
A ONLY
A INT B
B ONLY
A & B ALT
EXT
TIME
VOLTS
PART OF DM3010
EHT GENERATOR
BISTABLE – 2
INHIBIT FOR X–Y
A S/SHOT BISTABLE
A T/B BISTABLE
TRIGGER GATE
A RAMP GEN
HOLD OFF
B RAMP
A RAMP
DISPLAY BISTABLE ÷ 2
A/B ALT
B S/SHOT BISTABLE
B T/B BISTABLE
B RAMP GEN.
ALT PULSE GATE
DELAY COMPARATOR
TIME MEASURE BISTABLE
MEAS. TIME
MEAS. VOLTS
TIME MEASUREMENT COMPARATOR
VOLTS MEASURE BISTABLE

generator then runs either for its full period or until the end of the 'A' ramp, whichever occurs first, when the 'B' bistable is reset. The 'B' single shot bistable ensures that there is only one 'B' sweep during any 'A' sweep. The output of the 'B' bistable drives the Bright Up Amplifier to brighten the 'B' portion of the 'A' trace above the normal level. This mode is used to identify a portion of the trace for subsequent expansion in the B Only mode.

'A' INTENSIFIED BY 'B' (GATED)

This mode of operation is similar to 'B starts after delay' above, but the B timebase bistable is set only on the receipt of the first B trigger signal after the end of the set delay period, thus synchronizing the B sweep to the B trigger signal.

'B' ONLY

In this mode, the 'A' and 'B' timebase systems operate as for 'A Intensified by B' above, but the B sweep is selected by the X Select Switch and the trace is turned on only during the B sweep. The effect on the display is to select and expand the original intensified portion of the 'A' Intensified by 'B' trace to fill the full screen.

'A' AND 'B' ALTERNATE

This mode displays the A ramp and B ramp on alternate sweeps. The first sweep provides an A intensified by B trace, where the A sweep is selected for the X amplifier input, and the B ramp generator provides an intensified trace when the A ramp reaches the position set by the Delay control. On the next A sweep, the B ramp signal is selected to be fed to the X amplifier, and bright up is provided only during the period of B sweep. On this sweep, an additional shift signal controlled by the Trace Separation control is gated into the Y amplifer. This control allows the B trace to be separated from the A intensified trace by up to ±4cms.

4.1.6 X–Y MODE

When this mode is selected the timebase system is inhibited and the Sweep Select switch connects the A Trigger signal to the X Output amplifier as the X deflection signal. Trigger source selection allows the CH1, CH2, External or even Line signal to be chosen.

4.1.7. DIGITAL MEASURING UNIT

This optional addition to the 0S3500, DM3010, contains a digital multimeter which can operate independently to measure d.c. voltage, current or resistance. In addition it can operate with the 0S3500 to provide digitat readout of parameters displayed on the screen.

VOLTAGE MEASUREMENT

In this mode, the 0V of the DM3010 is connected to the CH2 shift voltage of the 0S3500 and an additional shift voltage is generated within the DM3010, determined by the v/t Control.

An electronic switch controlled by the Volt Measure Bistable selects as CH2 shift on alternate sweeps, either the normal CH2 shift signal or this additional offset signal. The effect is to produce two traces with an offset which can be set by the v/t control. The d.v.m. measures this voltage and is scaled according to the CH2 sensitivity chosen, to display the offset directly as a voltage.

TIME MEASUREMENT

In this mode, the 0V of the DM3010 is connected to the delay level set within the dual timebase system of the 0S3500. The v/t control determines an offset voltage which is applied to an additional comparator on the A ramp. The output from the normal Delay Comparator or that from the Time Measurement comparator is selected by the Time Measurement Bistable on alternate A sweeps as the signal to initiate the B sweep. The effect is to produce delayed B sweeps at two positions along the A sweep. The time difference between them is indicated as the voltage measured by the d.v.m. after automatic scaling according to the Time/cm set on the 0S3500.

In the 1/Time or Frequency mode of operation, the measured and reference voltages of the d.v.m. are reversed, inverting its reading for it to display the frequency equivalent to the selected time.

The control logic inhibits the simultaneous selection of Voltage, Time or Frequency measurement with Alternate mode of the timebase system to avoid the confusing display of 6 traces.

4.2. Y AMPLIFICATION

4.2.1 ATTENUATORS AND PRE–AMPLIFIERS (Fig. 6)

NOTE: The attenuators and pre-amplifiers in the Channel 1 (CH1) circuit are identical to those in Channel 2 (CH2). Accordingly, only the CH1 channel is described. The component numbers in CH1 have an equivalent component in CH2, the odd numbered components are in CH1 and even numbers in CH2.

The 'Y' input signal is applied via the BNC type socket on the front panel and routed to the A.C./D.C. switch S11, via a low value resistor, R51. In the D.C. selected mode, the signal passes directly to the NORMAL/ GROUND switch, S13, which when released passes the signal to the eleven position switched ATTENUATOR, 59. With A.C. selected, the input signal is routed through C51 and C53 before being applied to the attenuator, these capacitors forming a d.c. block.

Part of the attenuator is formed by three fixed networks, introduced into the input line in turn by selection from the ATTENUATOR switch. These networks introduce fixed attenuations of 1, 10 and 100. The unity network comprises C109, the X10 network is formed by C105, C107, C61 and R103. The X100 network comprises C101, C67, C103, C63, R81 and R101. All these networks have a wide frequency response.

After passing through the selected network, the signal is applied to the gate of f.e.t. TR101 via an input protection circuit comprising D101 and D103, and Zener diodes D105 and D107 with associated resistors and capacitors which reverse bias D101 and D103 under normal operation. TR101 is connected in the source follower configuration and its output is applied to the emitter follower TR103. The output from this impedance converter stage feeds the fixed, thick film, ladder network RN101.

The outputs from RN101 are selected by S9c. When the X1 network is selected, this wafer selects each of the five positions of the ladder network, giving 2mV/cm, 5mV/cm, 10mV/cm, 20mV/cm and 50mV/cm sensitivity levels at the first five positions of the Attenuator switch S9. On the 100mV, 0.2V and 0.5V/cm positions of the switch, the X10 fixed attenuator network is introduced into the circuit and only the last three positions of the ladder RN101 are selected, e.g. on the 100mV/cm setting, the X10 network is selected along with the 10mV/cm position on the ladder, giving 10 x 10mV = 100mV/cm. The next three positions give sensitivities of 1V, 2V and 5V/cm. These values are achieved by selecting the fixed X100 attenuator network and again the last three outputs from RN101 (10mV, 20mV and 50mV/cm).

Low voltage drift in the input circuit is achieved by applying the voltage at the wiper of R135 to the non-inverting input of bi-fet op-amp. IC101 at pin 3. The inverting input at pin 2 of IC101 has 90% of the input signal applied to it from the divider network R67, R69 in the input circuit. The op-amp is therefore comparing the output from R135 with 90% of the input voltage. Any different voltage is applied to TR105 base, which in turn varies the current into TR101 and alters the current into R135 from TR103. This loop then maintains the output potential at the emitter of TR103 to the signal input potential. R135 is adjusted to set the low frequency gain of the stabilization loop to match the gain of the direct wideband signal path via TR101 and TR103. D.C. balance of this stage is set by R117.

After attenuation the signal is passed to the differential pair TR107 and TR109 via ferrite bead L109. These two transistors form a differential cascode amplifier with TR111 and TR113. The gain of this circuit is determined primarily by the ratio between the value of R143 and the total value of R75, R77 and R13, the latter being adjustable as the Variable gain control. The Variable gain balance control R157 adds or subtracts current in the emitter of TR111 such that the d.c. voltage across R13 is zero. The differential output is fed to emitter followers TR115 and TR117, which feed a second differential amplifier TR119 and TR121.

The amplifier gain is set by R221, together with the fixed value resistors R223, R211 and R213 connected between the emitters of TR119 and TR121. HF compensation is provided by R215, R217, R219 and C145, C147 and C149. TR119 output is applied via R225 to a transistor switch pair contained within IC103. Similarly, TR121 feeds its output via R227 to a similar pair within the same package.

IC103 performs an inversion function on the two output signals under the control of the Invert switch S101. In the normal position of S101, the bases of IC103(a) and (c) are biased off, from the negative supply rail via R237 and R235 and the output signals pass through transistors IC103(b) and (d) to the channel switch without inversion. When S101 is in the Invert position, the bases of IC103(b) and (d) are taken to the negative supply rail via R237 and R239 and these two transistors are cut off. The output signal is then routed to the opposite channel. Potentiometer R231 provides the Invert Balance by altering the emitter current in transistors (a) and (b) in IC103, thus ensuring that the currents in the collectors of each transistor pair are balanced for both positions of S101. Two further outputs, from the amplifier TR119, TR121 are fed to the Trigger Pick-Off amplifier via R249 and R263. TR123 and TR125 form this differential amplifier, the purpose of which is to generate a trigger signal from the Y input. The output is routed from pin 141 by co-axial cable to the trigger circuit. R245 provides negative bias to balance the collector current of TR125 and so maintain the output across the 50Ω termination, R203, at Ov when the CH1 input is grounded. As stated at the beginning of this section, all the above circuitry for CH1 is duplicated for CH2. The equivalent circuit reference for CH2 is the even number following that for the component in CH1 and the differential signal output from CH2 is taken from IC104.

4.2.2. SHIFT SIGNAL GENERATION (Fig. 6)

The shift front panel control R11 determines the output of the differential pair TR127 and TR129 which is added to the signal output from IC103.

CHANNEL 2

A different arrangement is necessary for CH2 to provide for the DM3010 Voltage Measurement circuitry. The resultant shift current is fed from the collectors of TR128 and TR130 via R329 and R3301 to add to the signal current from IC104. The base of TR128 is held at fixed voltage (-6.1v) determined by the zeners D121, D122, the low value resistor R294 and D123. TR130 is driven via the attenuator network R290 and R289 from the emitter follower, TR131. TR131 is driven from signals provided by a two way analog switch IC105. This device has control signals at pins 12 and 13 determined by TR133 and TR134. Normally TR133 is turned off and TR134 is on. Pin 13 is high (-2.7v) and pin 12 is low (-7.3v). This provides a low impedance path between pins 1 and 2 and a very high impedance between pins 10 and 11. Hence the emitter follower TR132 controls the emitter follower TR131. TR132

derives its base voltage from the setting on the CH2 Y shift control R12 and this can vary over a 9.4V range, with the most negative voltage determined by R294 and D123. When DM3010 voltage measurement is selected, TR133 and TR134 switch on alternate timebase sweeps as determined by the bistable IC705a on the timebase assembly. The voltage at the emitter of TR132 is fed to the DM3010 shift amplifier via pin 5 of SKM. A voltage in the range of 0–4V added to the setting of TR132 emitter voltage is fed back from the DM3010 via pin 4 of SKM to pin 10 of IC105. The 0–4V setting is determined by the voltage shift V/T control on the DM3010. When pin 2 of IC105 is high the impedance path between pins 10 and 11 is low and the voltage shift signal from the DM3010 is fed to the base of TR131 to provide the Voltage Measurement Y shift trace. The setting of the DM3010 V/T shift gain is determined by R283 and preset control R284 between the emitters of TR128/TR130.

4.2.3. BEAM SWITCHING (Fig. 6)

Transistor switch arrays IC301 and IC302 are used to select the CH1 signal from IC103 or CH2 from IC104. Differential signal currents from IC103 (CH1) are applied at the emitters of two common emitter connected pairs in IC301. The bases of elements (b) and (c) are held at a fixed potential while the potential on the bases of (a) and (d) can be switched by the output of the beam switch bistable IC305b via emitter follower IC301(e).

If the logic level from $\overline{Q}$ of IC305b is high then the bases of transistors IC301(a) and (d) will be lower than those of (b) and (c). (a) and (d) will conduct to divert the output from IC103 to the -5V supply.

When the $\overline{Q}$ output of IC305b goes low then transistors IC301(b) and (c) will conduct and the CH1 signals will pass into the diode gate circuit D330, D331, D332 and D333.

The CH2 circuit operates in an identical manner. In this circuit the transistors form part of IC302, however because of the reversed connections to the collectors of these transistors, the logic level required from IC305b to achieve an output is reversed, e.g. a high on the input from IC305b will allow transistors (b) and (c) to conduct, and the CH2 signal is passed through to the diode gate.

When both S709 and S710 are selected, for SUM operation, a logic low is applied from IC305b as for a CH1 output but in addition a high is provided to transistor TR302(e) emmitter via D329 and R337. This input overrides the logic low input from IC305b at its base and gives a high output to transistors TR302(a) and (d) allowing both to conduct and CH1 and CH2 signals are applied to the diode gate. At the same time, D334 conducts and R335 and R331 provide an additional bias current to offset the doubled standing current of the two channel signals.

The control line from $\overline{Q}$ of IC305b is made low or high by resetting or presetting the bistable. When the CH1 push button switch, S109, is operated, the Preset input of IC305b at pin 10, is taken to ground. This causes the $\overline{Q}$ output at pin 7 to go low and CH1 is selected. When the CH2 switch, S710 is operated, the Clear input of IC305b at pin 14, is taken to ground via the return path from the now released CH1 switch. This causes the $\overline{Q}$ output at pin 7 to go high and CH2 is then selected.

Alternate channel switching is selected by operating the ALT switch, S711. The alternate pulse, from the timebase board is applied to pin 13 of IC303 and pin 1 of IC305a at the end of each ramp sweep. Since the Chop switch S712 is in the out position a ground is applied to pin 2 of IC303a from the S712 contact to ground. This logic low is inverted by the NAND-gate IC304c at pin 8. The resultant logic high, at pin 8, is applied to pin 12 of NAND-gate IC303d and the gate is thus enabled each time the input at pin 13 goes high. Pin 13 has applied to it the Alternate pulse from the timebase. Pin 11 of IC303d therefore provides an inverted pulse coincident with the end of timebase sweep. This output feeds pin 5 of NAND-gate IC303b which inverts the pulse again and clocks IC305b on the negative edge at the end of the pulse. The bistable IC305b $\overline{Q}$ output will therefore change state coincident with the pulse inputs from the timebase board, and select CH1 and CH2 alternately at each scan.

When the Chop switch (S712) is operated, the ground input is removed from pin 2 of NAND-gate IC303a. This gate then functions as a free-running relaxation oscillator in conjunction with the other NAND-gate IC303b, at pins 4, 5 and 6. Feedback is provided by C315, R354 and the circuit oscillates at approximately 1MHz The logic high level at pin 2 of IC303a, also at IC304c pins 9 and 10, is inverted and the resultant logic low at pin 8 is applied to pin 12 of IC303d. This prevents the Alternate pulse input operating the bistable IC305b since the NAND-gate IC303d is held high at pin 11. IC305b$\overline{Q}$ output at pin 7 therefore switches at approximately 500kHz and CH1 and CH2 are selected for display at this frequency.

The control line for the diode gate D330-D333 is applied from TR306 emmiter to the junction of D330 and D331. In Normal operation the line is held at logic low only if 'Trigger View' is selected does this line go high. When the input to the junction of D330 and D331 is held at logic low, both of these diodes are reverse biased and diodes D332 and D333 are turned on. The selected CH1 or CH2 signal from IC301 or IC302 can then pass via D332/R313 and D333/R316 to the grounded base amplifier TR303 and TR304. These two transistors form the driver amplifier for the delay line.

When the control line at D330 and D331 anodes goes to logic high, diodes D330 and D331 now conduct to select the Trigger view signal and diodes D322 and D333 are cut off to block the CH1 and CH2 output path to the amplifiers TR304 and TR303.

A chop blanking signal is generated by the common emitter amplifier TR307, fed from the chop oscillator output IC303b pin 6. This delivers a positive going blanking pulse to the Bright Up amplifier on the power supply assembly via R355 and a coaxial cable link.

The trigger view function permits viewing of the trigger pulse in lieu of either CH1 or CH2 when the Trigger View switch (S713) is operated.

The Alternate timebase pulse, as used for the CH1, CH2 Alternate function, is also fed to the clock input of IC305a at pin 1. This bistable is held reset, unless the Trigger View switch is operated, by a logic low at the Clear input pin 15. This logic level is derived from the -12V line via S713 and resistor R840. The Q output is therefore low and this is applied to emitter follower TR306. The resultant low at the emitter of TR306 is applied to the junction of diodes D330 and D331 in the diode gate circuit previously described and thus enabling the normal channel selection.

When S713 is operated to select 'Trigger View', the logic low is removed from the Clear input and the bistable IC305a is clocked by the incoming Alternate pulse at pin 1, its output states reversing on each pulse input from the timebase.

When Q goes high on the first clock pulse, $\overline{Q}$ goes low. This causes a logic high to be applied to the diode gate. Diodes D331 and D330 conduct and cut off D332 and D333 hence blocking the signal path of CH1 and CH2 outputs. At the same time, the $\overline{Q}$ output, a logic low at this time, is fed by emitter follower TR305 to the junction of a second diode gate formed by D303, D304 and D301, D302. This input biases diodes D303 and D304 off and D301 and D302 into conduction. The 'Trigger View' input applied via R328 and R326 is then allowed to enter the delay line driver stage. This alternate selection is repeated on each input pulse from the timebase board.

To prevent the 'Trigger View' function from operating when 'Composite Trigger' is selected, a contact on the 'Composite Trigger' switch (S508) connects the Clear input of IC305a to ground, thus restoring normal CH1, CH2 operation when this switch is operated.

The resultant current output from the channel selection and trigger view selection switching stages is applied to the grounded base stage TR303 and TR304 to drive the signal delay line.

A composite trigger waveform is derived from the beam switched CH1 and CH2 signals by applying a portion of these outputs into the composite trigger amplifier formed by TR301 and TR302. The resultant output is applied via a 50 ohm co-axial cable to the trigger board. Resistor R310 and preset R311 provide a 'Composite Trigger Balance' control.

4.2.4. 'Y' OUTPUT AMPLIFIER (Fig. 7)

CH1 and CH2 or 'Trigger View' signals are fed from the delay line into the emitters of the common base amplifier, TR400 and TR401, via R400 and R401 which terminate the delay line. The signals developed across the collector load resistors R406 and R407 and applied via emitter followers TR404 and TR405 to the bases of long-tailed pair TR402 and TR403. Frequency compensation is provided by the peaking network, R413-R416, C403-C406 in the emitter circuits. The two outputs pass through R417 and R418, which are shunted by C408 and C407 and are then limited by diode network D400, D401, D402 and D403, which prevent the output transistors saturating.

The limiting function is essentially achieved by the diodes D402 or D403 not conducting when the signal reaches an excessive level at their anodes. This limits the amount of signal fed to the shunt feedback amplifiers TR406 and TR407. In the normal (i.e. not Trace Locate) operation, current is fed from the +12V supply to the anodes of D402/D403 via the resistors R421, R422 and the parallel combination of R419 and R423. This provides the collector load currents for TR402 and TR403 and also the anode currents for D402/D403. A sink current is applied to the cathodes of these diodes via R426, R427 and the parallel network R429/R425 which also biases TR406 and TR407. If, for example, TR402 tries to conduct excessively and TR403 is almost cut off; then TR402 conducts more current than R422 can supply and D402 becomes reverse biased. The excess current demanded by TR402 is then supplied from the other load resistor R421 via D401. A similar situation exists with D403 and D400 when TR403 tries to conduct excessively. As a result, the signal to TR406 and TR407 is limited. When the Trace Locate switch, S400, is operated the limiting current thresholds are dropped by reducing the available source and sink currents to D402 and D403. This is done by disconnecting R423 from R419 and R425 from R242. The reduced current supply thus causes the trace to limit to approximately ±3cm, i.e. to remain on the screen.

When the Trace Locate switch is pushed, the -12V supply is removed from R464, the Intensity control. This assists with the bright up function as described in the bright up amplifier section.

The Y deflection signal from the diode clipping network is applied to the shunt feedback amplifier consisting of TR406 and TR407, with the gain determined by R428 and R429, the feedback resistors. R431 and C412 provide frequency compensation for TR406 and similarly R432 and C413 for TR407. The collector loads are formed by R436 and R437.

The outputs of TR406/TR407 are fed into the level shifting Zener diodes D404 and D405 and to the long-tailed cascode amplifier formed by TR408, TR409 and TR411, TR412. Frequency compensation is

provided by the networks R446, R447, R449, C422, C423 and C425 in the emitter circuits. R460, C435 and R448, C424 provide neutralization. The Final output signal is applied, via the peaking coils L402 and L403, to the 'Y' plates of the c.r.t.

4.3 TRIGGER

4.3.1 TRIGGER SELECTORS (Fig. 8)

The trigger source for Timebase A is selected by operation of one of the interlocked switches S508, S509, S510, S511 or S512.

The Composite CH1 and CH2 signals are generated at 50Ω impedance on the pre-amplifier board and fed via co-axial cables to S508, S509 and S510 respectively. The line signal applied to S511 is derived from a secondary of the supply transformer and fed via pin 603 and a potential divider R665 and R664. C584 removes any unwanted high frequency interference.

The External input signal is fed via a high impedance potential divider, R661 and R662 to S512. Frequency compensation for this divider is provided by C580, C581 and C582. C583 allows adjustment of the input capacitance.

The selected signal is passed via a link from pin 601 on the trigger source board to pin 507 on the main trigger amplifier board and into the coupling selection switch bank S501, S502, S503 and S504. These switches operate independently. The function of the Slope switch, S501, will be described later (section 4.3.2).

When D.C. only is selected the signal from pin 507 is routed directly through S504, S503, R559, S502 to the gate of TR501, the A trigger amplifier. When A.C. coupling is selected by S502, C543 is introduced into the circuit for wideband A.C. coupling. When L.F. Reject is selected by S503, a much smaller capacitor, C542 is introduced, allowing through only the high frequency components of the trigger signal.

When HF Reject is selected, R598 is introduced into the circuit with C540 to ground as a filter to reject high frequency components of the trigger signal. When the External source is selected, C540 alone is in circuit and the effect of R598 is increased by the high output impedance of the Ext. attenuator. When S512 is not selected, C585 is connected in parallel with C540 to maintain the same time constant with R598 along from a low impedance source.

The B selection and coupling circuitry is similar to that described above for A and is based on S513, S514, S515, S505, S506 and S507. This timebase does not have facilities for line source, somposite source or A.C. rejection coupling.

4.3.2. TRIGGER AMPLIFIERS (Fig. 8)

The input stage of the amplifier circuit is formed by f.e.t.s TR501 and TR502. Resistor R501 determines the input impedance of approximately 200k ohms.

Field effect transistors TR501/TR502 are a dual matched pair in a single package. TR501 acts as a source follower and TR502 acts as a constant current load through R505 which also provides drift correction.

The f.e.t. stage drives TR503, an emitter follower with two output paths; one from its emitter to the emitter of TR505, via R515 and out to the External X amplifier circuit, the other via R529 to the base of TR507, in the trigger amplifier.

For X-Y operation, the output passes through R515 to the emitter of the common base connected amplifier TR505. The output from the collector of this transistor is applied to emitter follower TR506. Resistor R510, R511, and R512 provide the emitter load, with shunt feedback from the junction of these two resistors back to the base of TR505. The circuit gain is thus approximately 2 and adjusted by R512. Resistor R514 provides an offset current into the base of TR505, to bias the output voltage at TR506 emitter at 2.0V. Capacitor C506 connected across the base collector junction of TR506 provides a high frequency roll-off to compensate for the delay introduced by the 'Y' Amplifier delay line. The value of this capacitor is determined during initial testing of the oscilloscope. The output from the emitter of TR506 is passed to the X-Y output at SKP pin 9 via R516.

When the X-Y function is not in use, an inhibit signal is applied from socket SKP pin 4. This is in the form of a -12V level applied through R517 to the cathode of D502. This diode is then made to conduct and draws current from R510, R511 and potentiometer R512, thus cutting off TR505 and preventing any output to the X amplifier circuit. With TR505 cut off, the tail current of TR503 will now flow through R515 and R513 in parallel with R507.

To prevent the trigger amplifier TR507/TR508 drawing current from R515 and affecting the X-Y output when X-Y is in operation, an additional inhibit signal of +12V is applied at socket SKP pin 1. This is passed via Zener diode D503 and R534 to the emitters of TR507 and TR508, cutting off this stage.

During normal trigger operation, the output from TR503 emitter is applied to the base of TR507. This transistor forms a differential amplifier with TR508. The base bias for TR508 (-0.8V) is provided by the network R524, diode connected TR504 and R525. This voltage is adjusted by potentiometers R520 and R522, via R521 and R523 respectively. R523 is the main Trigger level control, R521 provides additional bias to balance the amplifier such that switching the input coupling from D.C. to A.C. causes no change of trigger point on a symmetrical signal. The gain of the stage is controlled by R528, with frequency compensation provided by R527 and C507, C508.

Outputs from the collectors of TR507 and TR508 are applied to the base circuits of the subsequent differential amplifier stage, TR509 and TR510, via resistors R538 and R539 respectively. The gain of this stage is determined by the values of R540 and R541 and frequency compensation is provided by C518. This stage performs a trigger signal splitting function, producing two pairs of balanced outputs.

TR509 collector output is developed across R543 and R545. An output at the junction of these resistors is applied to the base of TR511, which forms half of the 'Trigger View' amplifier. TR510 collector output is similarly developed across R544 and R546 and the signal at the junction of these two resistors is applied to the base of TR512 which forms the other half of the 'Trigger View' amplifier. Signal outputs from the collectors of TR511 and TR512 are then passed to SKR. From here they form the 'Trigger View' input to the 'Y' amplifier circuit.

The gain of this circuit is determined by the value of R548 and frequency compensation is provided by R549 and C514. The collector currents of TR511 and TR512 can be balanced by adjustment of the preset 'TV Balance' potentiometer R552. This sets the 'Trigger View' display to the centre of the CRT, when the trigger level is in the middle of the trigger 'window'. A -12V supply is applied at the wiper of R552 via R553 from SKP, pin 6. When the 'Trigger View' function is not selected, this voltage is removed and TR511 and TR512 are therefore without emitter current thus cutting off the trigger view stage.

The main trigger path uses the outputs from the splitter stage TR509/TR510 which are fed directly from the collectors of these transistors. Transistor TR509 feeds the base of TR513 vai R558 and TR510 feeds the base of TR514 via R559. This differential amplifier forms the final amplifier stage prior to the schmitt trigger input.

Circuit gain is determined by the values of emitter resistors R562 and R563 and frequency compensation is provided by R556 and C516. The common tail current flows through R561 and R560 to the -12V rail and C517 de-couples the junction of these resistors to HF.

Transistor TR514 is biased such that its collector is at 3.9V, which is the threshold voltage of an Emitter Coupled Logic (ECL) input signal. A 'high' normally being at 4.4V and a 'low' at 3.4V.

The ECL line receiver package, IC501, is used as the Schmitt trigger circuit. The signal input is applied to the inverted output, pin 14, to the inverting input, pin 12.

The non-inverted output from pin 15 drives the two buffer stages IC501a and IC501b. The non-inverting input of IC501a is used while the inverting input of IC501b is used. The two outputs are commoned.

When the Trigger Slope switch S501 is set for negative slope, a positive bias is applied to the network R572, R573, R575 and R576, to enable IC501b and cut off IC501c, inverting the trigger output signal. Conversely, for positive slope, this bias is removed, IC501a is enabled, IC501b is cut off and the non-inverted trigger signal is transmitted.

The trigger amplifier of the B timebase is similar to that described above for A, but it does not have the XY or trigger view output stages. The input stage is formed by the source follower TR520 and emitter follower TR522. This drives the amplifier TR524, TR525 for comparison against the trigger level defined by R612 with preset R610 for balance. Subsequently, differential amplifier stages TR526, TR527 and TR528 and TR529 are used to drive IC502 as the trigger circuit buffer amplifier with slope selection as IC501.

4.3.3 TRIGGER DETECTOR (Fig. 8)

The buffered output from the trigger circuit is coupled by C536 into the trigger detector circuit comprising TR515, TR516, TR517 and TR518. The purpose of this circuit is to detect the presence of trigger signals, driving the l.e.d. indicator and controlling the timebase in the Auto mode. The square or pulsed waveform from IC501 is differentiated by C536, amplified by TR515 and differentiated by C533 to appear as a train of positive and negative going spikes at low frequency or a square wave at high frequency.

Each resultant negative transistion is coupled via D508 into the monostable TR516 and TR517. In the absence of input, both transistors are cut off. A single trigger signal or transistion will turn TR516 and have TR517 on for a period of approx. 30ms determined by C531, C532 and R587. The output from the emitter of TR517 turns on TR518 to energise the indicator D515 which is seen to flash. A continual succession of trigger signals above approx. 40Hz will hold the monostable in the on state and the indicator will be energised continuously. The additional output from the collector of TR518 is taken via R595 and SKP pin 3 to the timebase circuit. This is normally near to OV in the absence of trigger signals but goes low in the presence of trigger signals to inhibit the timebase from free-running.

4.4 TIMEBASE

4.4.1 A RAMP GENERATOR (Fig. 9)

Each ramp generator is controlled by a bistable which is turned on by a valid trigger or other signal to start a sweep and turned off at the end of each sweep to await the next start. The bistable for the A timebase is IC701b.

The triggering input, from IC501 on the trigger board, is applied to the Clock input of IC701b at pin 11. If the D input of IC701b is assumed to be high at this time, controlled by IC702c output at pin 15, then the Q

output at pin 15 of IC701b will go high and $\overline{Q}$ at pin 14 low on receipt of a positive edge clock pulse.

The Q and $\overline{Q}$ outputs of IC701b feed the bases of transistors TR702 and TR704, connected as a long-tailed differential amplifier. With the Q output high, TR702 conducts and TR704 is turned off.

The principal of operation of the ramp generator is the charging of a selected timing capacitor from a constant current source TR714. The linear voltage rise is fed into a buffer amplifier and before a ramp starts, a feedback loop stabilises this output to ground by drawing off a current via the fly back transistor TR710 which equates the charge current.

In detail, TR702 collector is coupled via R736 to the emitter of the fly-back transistor TR710. When TR702 is turned on, TR710 is cut off as TR702 draws its emitter current from R749. D713 and Zener diode D712 limit the reverse bias on the base emitter junction of TR710. As TR710 is turned off, the constant current source provided by TR714 starts to charge the timing capacitors C721 and C722 with C719 and C720 if selected. Selection of the timing capacitor and resistor value RT from the resistor network RN is done by the A TIME/CM switch S3. The timing capacitors C719 or C720 are brought into circuit by transistors TR707 and TR708 for the following conditions:- C719 is in circuit when a low timebase velocity range is selected by S3. In this position, S3 provides a positive voltage from the +12V line to the base of TR707 via resistor R753, which saturates TR707 and so connects one end of C719 to ground. In a similar manner C720 is selected on the mid range timebase velocities, S3 now providing a positive voltage via R754 to the base of TR708. To ensure that they are cut off when not selected, the bases of TR707 and TR708 are held at approx. -4V by R742, R746 and R745, R747 respectively. R758, R759 and D717, D719 are used to 'bootstrap' the output ramp to the collectors of the transistors TR707 and TR708, ensuring that they do not drop significantly below 0V when the timebase ramp voltage is near zero. Resistor R776 and capacitor C714 at the base of TR707 remove any charge remaining in C719 when switching to a higher velocity range.

The trimmer capacitor C722 allows calibration of the high velocity ranges when neither C719 or C720 are selected. Note that on the mid ranges when TR708 is on and TR709 is off, C719 remains in series with C720 and their values are chosen accordingly.

The charging current from TR714 is determined by the value of RT, selected by S5 and connected from its emitter to the +24V supply and the potention on its base. This base voltage is fed from the emitter follower TR715, as determined by the potential divider network R765, R766, R780, R760 and R769 and potentiometer R767. RR767 is used as the main TIME/cm calibration adjustment to set the timing currents accurately for the mid-timebase ranges when the close tolerance capacitor C720 is in circuit. TR713 is normally off but, like TR707, it is turned on when the low velocity ranges are selected and R716 is effective to allow calibration of these ranges. D716 is reverse biased when these ranges are not selected so that R716 has no effect on calibration.

The variable sweep speed control R7 operates via the components R768, D714, D715 and TR716. In the calibrated position, the wiper of the control connects pin 4 directly to pin 7, and the associated switch S5 is open. TR716 simply acts as an emitter follower defining current in R7 but not presenting an appreciable load to the sweep rate control level at the emitter of TR715. As R7 is turned away from its end stop, S5 closes to energise the UNCAL indicator D12. After a small movement along the track, the voltage between pins 4 and 7 will exceed the necessary drop across D714 and D715 and current will be drawn through R768. Further movement of the Variable control R7 will cause the current in R768 to exceed that in R746. TR715 will be cut off and the control voltage on the base of TR714 will rise under the control of R7, reducing the voltage across RT and hence reducing the charging current to slow the ramp rate as required.

The ramp voltage is monitored at the gate of fet TR717 acting as a source follower. TR718, in the same package, provides a constant current source for TR717. As the two fets are almost identical and the gate of TR718 is strapped to its source. TR717 is biased automatically for near zero gate-to-source voltage. The ramp output from TR717 is further buffered by emitter followers TR719 and TR720. The output from TR719 is coupled via D719 and applied to the X selector switch IC709b and via R718 to the Ramp Output socket on the rear panel. This signal is also applied via the divider network R729, R711 and R713 to the gate IC702a. When the emitter of TR719 reaches approx. +4.4V this gate switches to apply a clear signal to the A timebase bistable IC701b and complete the sweep.

With IC701b reset, TR702 is cut off and TR704 conducts. TR710 conducts as a constant current source to exceed the charging current from TR714 and the ramp voltage returns rapidly toward 0V, i.e. 'flyback' occurs. When the ramp output from TR720 reaches this level TR723 comes into conduction and its collector current diverts emitter current from TR710. TR722 and TR723 form a comparator and the loop stabilizes the ramp voltage ready to start the next sweep. TR711 conducts only as the ramp reaches its 0V level on fast flyback rates and prevents overshoot of the start point. The ramp output from TR717 is coupled to emitter followers TR719 and TR720 which are used to buffer the ramp output to the X amplifier and delay comparators IC710a and 710b.

4.4.2 HOLD-OFF (Fig. 9)

The hold-off circuitry is provided to enable the ramp generator to recover fully at the end of its sweep before another sweep commences. It also allows the 'X' Amplifier to stabilize. The period during which the timebase is prevented from triggering can be varied by operation of the HOLD-OFF control. This allows stable triggering from complex waveforms.

The hold-off system operates in a similar manner to the timebase ramp generator. It contains two constant current sources. TR751 charges one of the hold-off capacitors C710, C712, C713 as selected by the A TIME/cm switch S3. The other constant current source TR721 acts as a flyback transistor to discharge the hold-off capacitors. The voltage on the selected hold-off capacitor is buffered by TR712. The emitter current from the emitter follower TR719 flows through D719 and the potential divider R748 and R770. When the ramp output is rising and reaches about 2V (Approx. ½ ramp period) the potential across the junction of R748 and R770 exceeds the forward potential of D710 and the emitter voltage of TR721, thus turning the flyback source off. This enables the current source TR751 to charge the selected timing capacitor. C712 and C713 are selected by TR706 and TR705 in a similar manner to the timebase capacitors C719 and C720 described previously.

As the hold-off potential goes positive, TR712 is cut off and a logic low is applied to the OR gate IC702b. Positive feedback is applied via R727 and C706 so that a rapid transition occurs at the output of this gate.

The output of IC702b is applied to the NOR gate IC702c, at pin 13. Because the other input of this gate, at pin 12, is the Q output of IC701b, which is high during positive excursions of the timebase ramp then a logic high is fed from pin 15 of IC702c to the D input of IC701b. The Q output of bistable IC701b therefore remains high, since further clock pulses cannot change its state.

When the ramp has reached maximum positive (4.4V) and reset occurs as previously described, the flyback commences. As the flyback continues the ramp output voltage falls and at approximately 2V, diode D710, controlled by the voltage at the junction of R748 and R770 cuts off. This allows TR721 to conduct and discharge the hold-off capacitors via R737.

Variable hold-off is achieved by varying the emitter current of TR721 from the HOLD-OFF control on the trigger pcb via R741. This controls the ramp amplitude seen at the base of TR712 and so varies the hold off time. Delay periods of up to one timebase period can be achieved.

As a result of the hold off flyback transistor being switched off when the timebase ramp amplitude exceeds 2V, charging of the hold off capacitors C710, C712 and C713 continues until about half of the ramp flyback period has occured. When the ramp voltage has dropped below 2V the flyback current source conducts again discharging the hold-off capacitors. The discharge period continues well beyond the ramp flyback period until the voltage on the hold off capacitor has dropped sufficiently to turn on TR712. When the main timebase bistable IC701b switches over driving the Q output low at pin 15 at the commencement of the timebase flyback period, the output of the gate IC702c pin 15 drops low. This puts a low on pin 10 of IC701b, hence further clock pulses do not change the state of the bistable. At the end of the hold off period when TR712 has turned on, the output of IC702c pin 15 is brought high again via the signal from IC702b. This results in a high being applied to pin 10 of IC701b in readiness for the next trigger signal to start another ramp. A negative going signal edge from IC702c pin 9 to capacitor C773 provides positive feedback into the hold off circuit for a rapid switch off.

At the end of each sweep the emitter of TR703 goes positive and this transition is coupled through D711, R731 and C763 to produce a positive 'spike' at the input to gate IC707C. This inverts the impulse to generate a narrow low going pulse on its output which is distributed as necessary to switch control circuitry in the various Alternate modes. TC707b is normally enabled to transmit this pulse to the beam switching circuitry of the Y amplifier via SKU pin 715.

4.4.3 AUTO, SINGLE SWEEP AND X-Y (Fig. 9)

The timebase modes AUTO, NORMAL and SINGLE sweep are selected by the three interlocking switches S707, S706 and S708 respectively. Whereas in the NORMAL mode no timebase ramp will occur in the absence of trigger; in the AUTO mode the timebase free runs and produces a bright line trace.

When AUTO function is selected by depressing S707, the ground is removed from the Auto Bright Line input at SKS pin 3. This allows the junction between R720 and C706 to follow the control signal from the trigger detector circuit from SKS pin 3. In absence of trigger, D706 is cut off. D707 and D749 have their anodes taken to the +12V rail via R728 and when IC702b output at pin 14 is low, current will flow from R728 to ground via R724. This causes a logic low to appear on the preset input pin 12 of IC701b via diode D707 and R719.

At the end of the hold-off period, pin 14 of IC702b goes high. The current flowing in R728 will then pull the Preset input of IC701b high via D707. The Q output of IC701b is therefore driven high and the ramp sweep restarts without any trigger applied. When a trigger signal occurs, the trigger detector operates. TR518 on the trigger circuit turns on the 'TRIGGER' LED and also removes current from R728 via D706 and R720. This has the effect of making the preset input of IC701b

go low. The timebase will only sweep in this condition when a trigger signal clocks the bistable IC701b.

In the NORMAL mode of operation, the ground provided by S707 prevents the Preset input of IC701b from rising, by returning the current in R728 to ground via D706 and R720.

When the SINGLE SWEEP button S708 is depressed, both S706, the NORMAL switch and S707, the AUTO switch, are released. This inhibits both normal and auto triggering of the timebase. S708 operates as a spring return action switch without any latch action. Each depression of S708 will cause the timebase to be armed in readiness for a trigger signal, which when given will cause the timebase to make one sweep and then reset.

With S708 in the released position, C701 charges via R701 from the +5V rail. On pressing S708, this charge is applied to the Preset input of IC701a at pin 5, setting the outputs to Q high and $\overline{Q}$ low. The Q output at pin 2 of IC701a is applied to the emitter of TR701. Because the base of this transistor is held at approximately 3.3V by the network D702, R710 and R712, it conducts and passes current to the ARMED led via R709 and SKV12. The low $\overline{Q}$ output at IC701a pin 3 is applied via R703 to pin 4 of OR-gate IC702a. The other input to this gate is applied from the reset line to pin 5 which is normally low except at ramp reset, therefore the output at pin 2 will be low to the clear input of IC701b.

IC701b therefore awaits a trigger pulse to initiate a ramp with the single shot armed l.e.d. illuminate. When this occurs and the timebase has completed the ramp, IC701b changes its state to Q low (pin 15) and $\overline{Q}$ high (pin 14) in the normal way to commence the fly-back. This action then clocks a logic low to IC701a since the D input is permanently low on pin 7. The Q output at pin 2 of IC701a then drops low and the ARMED l.e.d. is turned off. IC701b is then held reset by IC701a. $\overline{Q}$ signal at pin 3 via the gate IC702a. The bistable IC701a can then be prepared for another sweep by pressing the 'ARM' button S708 once again. R703 and C775 from a low pass filter to prevent narrow spikes from IC701a resetting IC701b if S708 is pressed during a sweep.

When the timebase is in the AUTO or NORMAL modes, IC701a is held preset by diode D701 thus disabling the single shot function.

It is necessary to inhibit the 'A' ramp generator during the X-Y mode of operation. When the X-Y switch S705 is depressed, +12V is applied to the anode of D705 via R716. This voltage is clamped to +5V by D705 and is applied via R714 and D704 to pin 2 of IC702a. This pin is directly coupled to the Clear input of IC70lb, the timebase bistable, and holds this circuit in a permanent reset state.

4.4.4. DUAL TIMEBASE OPERATION (Fig. 9)

In the 'A Intensified by B', 'B' only and 'A & B Alternate' modes, the B timebase is initiated at a selected point during the A timebase sweep as set by the DELAY control. The B timebase may be initiated in two different ways, the simplest mode being B STARTS AFTER DELAY, which is set by S516 on the B TRIGGER LEVEL control, R612. In this mode, the setting on the DELAY control vernier determines directly the start of the B ramp. The B timebase may also be used in the 'B GATED' mode where the B timebase is merely armed on reaching the DELAY setting and awaits a trigger pulse from the B trigger amplifier before a B sweep commences. The delay period is generated as a portion of the A sweep period to the delay comparator circuit.

The A ramp is fed from the emitter of TR720 to the dual comparator IC710a and IC710b, via R897 and R898 to pins 12 and 5 respectively. The bistable IC705b is only functional if Time or 1/Time measurement is required while the DVM option DM3010 is fitted. Normally this bistable is held preset by a shorting plug on SKU pin 6 holding pin 10 of IC705b at 0V. This allows only the comparator IC710b to function since IC710a strobe is held low on pin 9. The DELAY control R5 on the front panel has exactly 4V set across it by the resistors R916, R917 and preset control R915. R917 has only about 80mV across it to act as a back-off voltage for the DELAY control to allow for various offsets in the comparators and timebase ramp generator.

The voltage at the wiper of R5 is fed to the unity gain buffer IC706 at pin 3. The output at pin 6 is then fed to the inverting input of the comparator IC710b at pin 13. When the timebase ramp has risen to the potential set by the DELAY control, the output of IC710b rises quickly to about +3.0V. R887 is used to provide some positive feedback which allows the comparator to snap over cleanly when the desired level is reached. The output from IC710b pin 1 turns off transistor TR746 by diverting the emitter current in R893 to D745 and R895. The collector of TR746 is only allowed to rise to +4.4V (ECL LOGIC HIGH) by the action of R890. The components D744, D745, C754, C755, R894 and R895 are relevant only when the DM3010 option is used. They introduce a delay of only a few nanoseconds to compensate for any differences in group delay between the two comparators. Section 4.7 covers the operation with DM3010 in full detail.

If the B STARTS AFTER DELAY condition is selected on the B TRIGGER LEVEL control (R612 and S516) then the input on pin 7 of IC703b is low. TR732 is switched off, providing a high input to gates IC703c and IC703d on pins 11 and 12 respectively. Since gate IC703c is turned on, its output at pin 14 will stay low and cannot pass trigger signals from the B Trigger Amplifier. The output of gate IC703d pin 9 goes high, which is applied to the D input of the B timebase bistable, IC704a, at pin 7. The positive signal edge from the

comparator IC710b via TR746 then passes through the two NOR gates IC703a and IC703b to emerge at the IC703b pin 3 and provide a positive edge trigger to clock the bistable IC704a at pin 6. This action initiates the B ramp.

When the B trigger amplifier is to be used in the 'B Gated' mode S516 on the Trigger pcb is closed, applying a high to IC703b pin 7 and at the same time turning on transistor TR732. This puts a low to the inputs of gates IC703c (pin 11) and IC703d (pin 12). Any trigger pulses from the B Trigger Amplifier will now pass through gate IC703c, becoming inverted as they do so. The output of IC703c pin 14 is fed to the clock input of IC704a pin 6. However, since the D input is low (pin 7) and the bistable, IC704a, is reset its state remains unchanged. When the comparator output IC710b rises as the ramp reaches the voltage preset by the DELAY control, the gate IC703d pin 13 is driven high via TR746. This raises the D input of IC704a high and enables the bistable to be clocked upon receipt of a trigger pulse and so start the B ramp generator.

Note that the gate IC703c inverts the trigger pulses and in order for the trigger to have the correct polarity the +/– TRIGGER SLOPE switch, S505, on the Trigger p.c.b. is wired in a reverse fashion with respect to the A Trigger Amplifier.

4.4.5 B RAMP GENERATOR (Fig. 9)

The B ramp generation system with its start point stabilization and hold-off circuit is very similar to that already described for the A Timebase. It does not include Variable Hold-off or Auto facilities but the detailed circuit description will not be repeated in this section, unless it is significantly different. When the bistable IC704a changes state to initiate the B ramp the Q output goes high (pin 2) and $\overline{Q}$ (pin 3) goes low. These two outputs are directly coupled to the bases of transistors TR724 and TR725. TR724 is therefore driven on and TR725 off. TR724 is coupled via R801 to the emitter of the flyback transistor TR727. This allows TR724 to draw the emitter current from TR727, thus turning it off. The constant current charging transistor TR738 then charges the timing capacitors C742, C746, C740 and trimmer C741 as selected by transistors TR728 and TR729 under the control of the B Time/cm switch S4. This switch also selects the current defining resistor RT in the constant current generator TR738, TR739 and TR740.

The potential at the timing capacitors is buffered by the source follower TR736 and emitter follower TR735 to provide the B ramp output.

The ramp output from TR735 is applied to pin 7 of OR-gate IC702 via R793 and HF compensation network R792, C735. These components together with R791 determine the switching point of IC702 and ensure it occurs at the 4.4V maximum excursion of the ramp. When this occurs, the output of IC702 goes high and applies this logic level to the Clear input of IC704a at pin 4. The Q and $\overline{Q}$ logic levels on this bistable are then reversed, switching the conduction states of TR724 and TR725, causing the ramp to reset.

During the waiting period before the B ramp commences, the output from TR735 is held at 0V by the action of TR733 which acts as a sweep start stabilization control. The emitter of TR733 is connected to 0V via the low value resistor R820. When the emitter of TR735 reaches 0V at the end of the flyback period, some of the current through R825 flows in diode D735 and thus turns on TR733. TR733 then controls the current in the flyback current source, TR727, at its emitter such that the voltage at the emitter of TR735 is maintained at 0V. TR734 in the emitter circuit of TR735 function as a diode to compensate for the voltage drops across D735 and the base-emitter of TR733. R824, R821 and C749 prevent overshoot on flyback in a similar manner to R756, R757 and C716 in the A ramp generator circuit.

When the timebase bistable IC704a is reset, the $\overline{Q}$ output at pin 3 goes high. This then clocks the single-shot bistable IC704b at pin 11. The $\overline{Q}$ output of IC704b therefore goes high because the D input at pin 10 is connected to ground. The high at $\overline{Q}$ is fed to the Clear input of IC704a at pin 4 and this prevents further triggering of the 'B' bistable.

When the 'A' ramp has completed its sweep the 'A' timebase bistable IC701b has a logic high at the $\overline{Q}$ output on pin 14. This high is applied to the Preset input of IC704b at pin 12, reverting the $\overline{Q}$ output at pin 14 to a logic low which is applied to the Clear input of IC704a, enabling this bistable to switch again on the next trigger pulse.

If 'A' only is selected, the 'B' timebase must be inhibited. This is accomplished by applying +5V to the anode of D734 when the 'A' only switch (S701) is depressed. This logic high holds the Clear input of IC704a at pin 4 high and therefore inhibits the 'B' bistable.

4.4.6 X MODE SELECTION

The three way analog switch IC709 is energized as necessary to select the A ramp signal, the B ramp signal or the X-Y signal to drive the X amplifier. Selection of A or B is derived from the state of bistables IC708a and applied to IC709 via TR743, TR744.

When A only is selected by S701, D721 conducts via R852. D722 clamps the Clear input to IC708 to 0V. With Q low and $\overline{Q}$ high, TR743 is turned off and TR744 is turned on. IC709b is energized, selecting the 'A' ramp. Similary when 'A Intensified by B' is selected by S702, 0V is applied directly to the Clear input of IC708a with the same result.

When 'B' Only is selected by S703, 0V is applied directly to the preset of IC708a. Q is high, $\overline{Q}$ is low. TR743 is turned on and TR744 is turned off, enabling IC709c to select the 'B' ramp.

When 'A and B Alternate' is selected by S704, the Preset and Clear inputs to IC708a are both high and this bistable is clocked at the end of each A sweep by the signal from IC707c. In all Y modes except 'CH1 and CH2 Alternate' the Preset into IC708b is energized and the Q output provides a high input to the J and K inputs of IC708a. The latter then switches state at the end of each A sweep, selecting 'A' and 'B' ramp signals on alternate sweeps.

In the Y mode 'CH1 and CH2 Alternate' switch S711 grounds the cathode of D743. TR748 is turned off removing the Preset from IC708b. This now forms a ÷ 4 circuit with IC708a and the X selection switches are driven to allow two consecutive 'A' sweeps followed by two consecutive 'B' sweeps. Meanwhile the beam switch in the Y amplifier chain is alternating between CH1 and CH2 to provide the required 4 trace display.

When 'A and B Alternate' is selected, trace separation is required. Operation of S704 removes the bias via R874 holding TR745 on. This is now switched in parallel with TR744 under the control of IC708a to enable IC709a on each 'B' displayed sweep. The bias set by the TRACE SEPARATION control R4 is applied to TR742 to modify the differential output current from the transistor pair TR743 and TR741. These signals are fed into the Y signal path.

In the X-Y mode S705 is operated. IC709d is enabled directly to select for X deflection the X-Y signal from the A Trigger Amplifier. Current in R853 via D725 and D726 ensures that both the Preset and Clear signals are applied to IC708a. Q and $\overline{Q}$ are both high, inhibiting both the 'A' and 'B' signals.

4.5 X OUTPUT AMPLIFIER (Fig. 10)

The ramp input from the timebase via IC709 is applied to the commoned base connections of TR810 and TR812 via R929. These transistors, with TR809 and TR811 form two long-tailed pairs. Transistors TR810/TR809 forming one, TR812/TR811 the other.

The opposite commoned base connection of TR811 and TR809 is fed with the X shift voltage from the emitter follower TR815 via R979. The base of the emitter follower is connected to R965 which forms a potential divider with R967 and R966 operated by the COARSE and FINE shift controls. Long-tailed pair TR810/TR809 has a 'tail' circuit comprising R962, R963, R961 and 'Set X1 gain' pre-set potentiometer R960. The 'tail' circuit of TR812/TR811 comprises R759, R958, R956 and 'Set X10' pre-set potentiometer R957. Resistor R928 and C831 across these last two resistors provide HF peaking.

The Long-tailed pair TR812/TR811 have their 'tail' current provided by the constant current source, TR813. The voltage at the base of this transistor is derived from the +24V rail by the potential divider R968 and R970. TR813 emitter is connected to the anodes of D812 and D813 via R969 and 'adjust on test' component R971 in parallel with it. The cathode of D812 is taken to -12V when S705, the X-Y mode switch, is operated. Similarly, the cathode of D813 is returned to the same potential when the X10 MAGNIFICATION switch is operated. When either diode cathode is taken to -12V the emitter of TR813 can draw current, enabling the long-tailed pair TR812/TR811.

A connection is also made from the anodes of D812 and D813 to the base of TR814 which supplies the 'tail' current for the other long-tailed pair TR810/TR809. A negative voltage applied at the base of TR814 will cut this transistor off and the associated long-tailed pair TR810/TR809 will be inhibited. In the absence of the negative bias TR814 is held in conduction by the potential divider R974, R975 and R976 to the +24V rail. Hence applying -12V via either D812 or D813 enables the long tailed pair TR811/TR812 to give X10 X expansion or allowing D812/813 to float enables TR809/TR810 to give X1 X gain. TR806 and TR808 operate as emitter-follower buffers to the common emitter stage TR805 and TR807 respectively. The remaining part of the X amplifier now operates as two independent shunt feedback amplifiers, each driving an X plate. TR803 forms a cascode stage with TR805 as also does TR804 with TR807. The collector loads of TR803 and TR804 are the constant current sources TR801 and TR802. Shunt feedback in the amplifier section TR801, 803, 805, 806 is applied via R938 together with the capacitor 'T' network C814, C818 and trimmer C816 applying HF compensation. This capacitor network operates in a way equivalent to the effect of a very low capacitance variable trimmer across R938. A similar feedback network, R944, C813, C815, C817 in the other amplifier half TR802, TR804, TR807 and TR808. The two amplifier halves differ in that TR805/TR806 and TR807/TR808 are PNP/NPN and NPN/PNP respectively. This enables the transistors TR805 and TR807 to provide maximum current drive to the output stages during the ramp period. Accordingly, therefore, the stage TR801/TR803 produces a positive going ramp signal at the commoned collector point, whereas that on the stage TR802/TR804 is negative going. The constant current sources TR801 and TR802 are provided with HF current boost via C807/C808 and C805/C806 respectively. This current drive is provided from TR805 and TR807 and the charge on the capacitors is recovered during the return transient via resistors R930/R941 and R931 respectively.

Components C821, R939, C810, L702 and C820, R943, C811, L701 are used to provide HF stability to each amplifier circuit. The current sources TR801 and TR802 are provided with bias voltage derived from the zener D801 and the bleed resistor R937, with C802 and C822 used for decoupling. This resistor is also used to provide current for the zener D802 which biases TR803.

The commoned emitters of TR805 and TR807 are held at the fixed potential of +7.5V provided by D803, C829

and R946. Hence the voltages at the bases of TR806 and TR808 are also fixed at this value and are virtual ground points. Current drive to these virtual ground points from the common emitter amplifiers TR809–TR812 described previously is fed via the diodes D806 and D807. Diodes D806–D811 are used in a current limiter circuit to prevent the output transistors TR801 and TR802 from saturating. The operation is best described by considering the case when TR812 is fully on and TR811 fully turned off. This would be the case when the timebase ramp is almost complete and an expanded trace has shifted well off to the right of the c.r.t. screen. TR812 emitter therefore takes all the current provided by the constant current source TR813. The current from the collector which normally flows through D806 to the base of TR806 would be sufficient to turn TR806 off and cause TR801 to saturate. However, because TR811 is not conducting the potential across R955 turns off D807, and the excess current from R955 bleeds through D810 and D811 to the collector of TR810. This prevents TR806 from being turned off and so limits the voltage at the junction of TR801 and TR803 from exceeding +135V. At the same time the voltage at the junction of TR802 and TR804 will be low, and since D807 is turned off, TR804 is prevented from saturating by the action of the current bleed through R951. TR804 normally limits at about +25V. A similar limiter circuit for the other amplifier half exists using D806, D808 and D809 which becomes effective prior to the start of trace on the left hand side of the c.r.t. display.

The TRACE LOCATE is achieved by the circuit R948, R949, D804 and D805. Normally D804 and D805 are reverse biased, with the result that no current flows in R948 and R949. When the TRACE LOCATE button is pressed +12V is applied to D804 and D805. This causes current to flow in R948 and R949 and divert some of the current from flowing is the virtual ground points at the bases of TR806 and TR808. As a result, TR806 and TR808 run out of drive current while the trace is still on the screen and the trace limits prematurely.

4.6 POWER SUPPLIES (Fig. 11)

The A.C. supply is applied to the primary windings of transformer T1 via the voltage selection switches S15 and S16, fuses FS1 and POWER switch S1. S15 connects the primary windings in series or in parallel, while S16 introduces an additional 20V tap as required. Multiple secondary windings provide low voltage a.c. inputs to the d.c. supply generation circuits. Secondary windings are also provided to supply 6.3V r.m.s. a.c. for the heaters of the c.r.t. and an a.c. input to the Trigger Amplifier circuit for use as described in Section 4.3.1.

4.6.1 LOW VOLTAGE SUPPLIES (Fig. 11)

+5V D.C. SUPPLY

This supply is derived from the output of bridge rectifier BR1002 supplied from T1. An additional a.c. output is also taken from this winding to supply the 'External DVM' facility.

The +9V unregulated output from BR1002 is applied to the voltage regulating integrated circuit IC1003 after smoothing by C1025. The voltage output from the regulator is determined by the ratio of R1049 and R1050. This ratio is such that 5V is obtained at the output. C1026 provides additional smoothing and de-coupling and diode D1023 protects the regulator IC in the event of the +5V output shorting to a negative rail. Fine adjustments of the output voltage of this supply can be made by selection of the Adjust on Test (A.O.T.) resistor, R1054.

–12V D.C. SUPPLY

A further seconday winding of T1 supplies the bridge rectifier formed by D5, D6, D7 and D8. The d.c. output from this bridge is applied to the reservoir capacitor C3 and the voltage regulator IC1002. The ratio of resistances of R1047 to R1048 is in this circuit adjustable by potentiometer R1051 and this preset is set to give 12V at the output of the regulator. This output is smoothed by C1023 and the positive side is connected to 0V. As a result, the un-grounded end of C1023 is therefore at -12V and this point forms the supply rail. Diode D1022 protect IC1002 in the event of the -12V output shorting to a positive supply rail.

The same secondary winding drives D9 and D10 which with D5 and D8 form a further bridge rectifier to generate an unsmoothed full wave rectified supply to drive the graticule illumination lamps. The actual voltage applied to the lamps is controlled by the potentiometer R466 and the emitter follower TR413.

+12V SUPPLY

Diodes D1, D2, D3 and D4 form a bridge rectifier for this circuit. Smoothing is provided by C2 and 18V is thus provided for voltage regulator IC1001. The output voltage is adjusted by R1052 to give +12V. The circuit action is identical to that described for the -12V supply but in this case the negative side of the stabilised supply is grounded.

+75V AND +150V SUPPLIES

These two supplies are derived from a single secondary winding, one end of which feeds a half wave rectifier D1018, giving the 75 volt output, and a voltage doubler circuit C1021, D1011, D1010, C1019, giving the 150V output. This end of the winding is made to swing ±75V about ground by the action of the bridge rectifier and C1017 connected between the low voltage end of the winding and ground. This allows the low voltage end to swing about ground by ±V where V is the voltage on C1017. Since the secondary winding supplies current to the 75V and 150V loads this tends to charge C1017 via BR1001. The voltage across C1017 is adjusted to maintain a constant 75V output by the conduction of TR1006. When the low voltage

end of the secondary winding swings negative, diode (a) in BR1001 is turned on, and the base of TR1006 is at its most negative value (approx. -1.5V). If the 75V bias is high then the 75V zener D1009 momentarily conducts thus removing charge from C1016. As a result, the base emitter voltage of TR1006 drops, which reduces current conduction in TR1006, and causes the voltage across C1017 to rise. This reduces the swing at the high voltage end of the secondary. If the 75V bias is low, D1009 does not conduct, consequently, C1016 charges continually via R1042 and TR1006 conducts more current causing the output voltages to increase.

+24V SUPPLY

This consists of a 12V regulator with its low terminal connected into the +12V rail. Feedback input at the junction of R1031, R1029 is compared with the references (generated internally at pin 4) applied to pin 3. The supply voltage for this regulator is derived from the +75V line by R1027 and the 18V zener D1008 connected to the +12V line. The +24V output from IC1004 at pins 1, 6 and 10 is fed via SKD pin 3 to the timebase circuit. C1006 provides output decoupling and D1012 protects IC1004 against a short circuit to ground by loading down the +12V line.

4.6.2 E.H.T. SUPPLIES (Fig 11)

The e.h.t. supplies for the grid, cathode and p.d.a. of the c.r.t. are supplied by a high frequency oscillator or inverter driven from the +12V and -12V supplies. Transformer T1101 is the e.h.t. oscillator transformer driven by transistor TR1103 biased to class C through the feed back winding 4 and 5 at a natural oscillating frequency of approximately 30kHz. Regulation of the -1.5kV supply is provided by a feedback control loop formed by TR1102, TR1101. The amount of drive and thus the magnitude of the e.h.t. output voltage, is determined by the base drive of TR1103 which flows through the feedback winding 4 and 5 of transformer T1101. As point 4 goes positive, increasing the conduction of TR1103, point 5 goes negative and C1105 charges negatively via D1105 and R1112. As a result the next pulse of output current from TR1103 will be less than the preceeding one and the e.h.t. output will also be smaller unless the charge in C1105 is restored.

The average charge on C1105 is controlled by the collector current of TR1102. If this current is sufficient then C1105 will not discharge, the required current being provided by the transistor. Transistor TR1102 is controlled by an error amplifier formed by TR1101. The reference voltage for this amplifier is derived from the +12V rail via R1105, R1106, R1103 and the error voltage is applied from the -1.5kV output via R1125 to the base of TR1101. The action of the circuit is such that a current balance is achieved at this base.

If the -1.5kV output at the c.r.t. cathode becomes less negative, TR1101 conducts more, increasing the base drive to TR1102 and increasing the current in the output transistor, TR1103, due to C1105 being charged positively. If the -1.5kV output becomes more negative, i.e. the voltage is too high, then TR1101 conduction is reduced. This in turn reduces the drive to TR1102 which allows the charge on C1105 to go negative and thus reduce the output voltage.

Diode D1103 in the emitter of TR1101 is always conducting and provides temperature compensation for this transistor, with the emitter current provided by R1114. Diodes D1101 and D1102 at the base of TR1101 protect the base-emitter junction. Preset resistor R1106 functions as the 'Set e.h.t. control'.

Resistors R1101, R1102 and diode D1104, in conjunction with the choke L1101, form a current limiting circuit. Under normal operating conditions the current through L1101 is approximately 250–300mA. If this should increase beyond this value, the voltage drop across L1101 will cause the decoupled +12V supply at the emitter of TR1102 to reduce to the point where D1104 becomes forward biased by virtue of the voltage across the potential divider R1101 and R1102. This diode then shorts out the error amplifier circuit and breaks the feedback loop so causing and effective current limit.

The secondary of the e.h.t transformer T1101 drives two separate voltage multiplier circuits. The first circuit is fed from point 8 on the transformer and comprises a voltage doubler formed by C1114, D1111, D1112 and C1115. The resultant output voltage at the junction of R1123 and C1115 is 1.6kV which is smoothed by C1116 after being dropped to 1.5kV by 100V Zener diode D1114. This is the point fed back as the error voltage to TR1101 and is fed via R1120 to the cathode of the c.r.t. holding this at a fixed potential.

An additional voltage doubler circuit C1109 D1107, D1108 and C1111 is driven from the same tap, pin 8, of the transformer but its output is referred at D1107 not to 0V but to the output potential of the bright-up amplifier, driven via emitter follower TR1104. If the emitter of TR1104 is near 0V, the voltage doubled supply, used to drive the grid of the c.r.t., would be at -1.6kV. That is the same as the output from D1112 and so more negative than the cathode by approximately 100V, the voltage across D1114. Thus the c.r.t. will be cut off. The grid is actually fed from R1119 which allows its potential with respect to the cathode to be adjusted to the point of cut off. As the output of Bright-up amplifier, decribed in Section 4.6.4, goes positive, the grid supply from D1108 will follow and the d.c. level fed to the grid via R1118 and R1039 will rise accordingly. However, the bypass capacitor C1015 will apply the transition rapidly to the grid. As this electrode moves positively with respect to the cathode the beam of the c.r.t. is turned on.

The third output from the e.h.t. oscillator is taken from pin 10 of the high voltage secondary winding and applied to a X5 multiplier module to generate +10.5kV which is applied to the p.d.a. mesh of the c.r.t.

4.6.3 TUBE CONTROLS (Fig 11)

A potential divider chain R1124, R475, R469 and D407 is connected from the -1.5kV cathode supply to 0V. R475 is the FOCUS control and the wiper of this potentiometer is connected to that electrode. The geometry or I.P.S. electrode is taken to the wiper of a potentiometer R473 connected from D407, approximately -91V, and +150V via R477 and R474. The astigmatism or A3 electrode is connected to the wiper of a potentiometer, R472, connected between -12V and +150V via R474.

The heater of the c.r.t. is supplied directly from its own winding on the supply transformer but its mean D.C. potential is held at the cathode potential by R6.

Minor misalignment of the deflection plates can prevent the trace from aligning with the graticule lines and a correction or trace rotation coil is fitted. Current through this is set by R467 and driven via emitter follower TR414 from the +12V and -12V supply lines. The presence of D408 allows the correction current to be adjusted through zero but the connections to the coil must be reversed if a large correction current is required.

4.6.4 BRIGHT UP AMPLIFIER (Figs. 9 & 11)

The function of the bright-up system is to turn the trace on to the level set by the INTENSITY control during each normal sweep and on continuously in X-Y mode. In the 'A intensified by B' mode, additional bright-up is applied during B portion of the A sweep. The system is based on a shunt-feedback amplifier and responds to the algebraic sum of signals derived from the INTENSITY control, the A Timebase Bistable, the B Timebase Bistable and external Z mod. input. An over-riding blanking input can be applied from the Chop Oscillator.

The amplifier is formed by TR1002 and TR1003, with shunt feedback via R1019 from the collector output of TR1003 to the virtual ground at the base of TR1002. TR1004 provides a constant current load for TR1003 with additional high frequency drive to the output via C1004.

In the blanked condition D1004 is reverse biased and R1016 and R1019 determine the output level at approximately +5V. Subsequently, current applied via D1004 will drive the output voltage positive. Full bright-up occurs with approximately 2mA in D1004 and the output at approximately +55V. When blanked, the current from the collector of TR1001 is 4mA. 2mA is drawn through R1014 leaving 2mA in D1003. This exceeds any current via R1013 from the INTENSITY control R464.

In the normal 'A' sweep, -2mA is drawn through R1002, reducing the collector current in TR1001 to 2mA. With no current in D1003, the current in D1004 is controlled by R464, i.e. the bright-up is controlled by INTENSITY as set. This condition applies also in the X-Y mode and during the A or B sweeps of 'A and B Alternate' and 'B' only modes.

In the 'A Intensified by B' mode, the current in R1002 is less than 2mA during the A sweep, increasing to 2mA or more during the B sweep. The amount by which this current is less thatn 2mA is determined by the preset Contrast control R850. Thus the resultant bright-up is determined both by the Contrast and Intensity settings.

In the Chop mode of operation, a positive drive is applied to pin 1014 during each chop transistion. Current through R1011 is applied via D1006 to exceed any current in D1004, blanking the trace as required.

A positive voltage applied to the Ext. Z mod. input will drive current via R1001 and D1001 to provide blanking.

The control currents via R1002 are derived from the timebase circuit as the summed currents from R561, R860, R859 and the collector of TR750.

In 'A' only, with S701 operated 2mA flows through R851 and D729 into the emitter of TR749. Since the bistable IC708a is in the Cleared state for this mode, TR750 is biased into conduction by the high $\overline{Q}$ output. The 2mA current from TR749 collector flows through this transistor and balances an equal and opposite current provided by R861. Before the A Timebase commences to sweep, the voltage at the emitter of TR703 is the same as that at the virtual ground blanking input Pt. 708 (i.e. 3V) and no current flows through R860. Also no current flows through R859 from the B Timebase. As a result no current drive is applied to Pt. 708. When the A ramp starts the emitter of TR703 drops to approximately 0V and a -2mA current flows through R860 which enables the Bright-up amplifier.

In the 'B' only mode, with S703 operated, there is no current in TR749 and hence none in TR750. Before the start of the A sweep, R861 defines +2mA into pin 708. When the A sweep starts, this is offset by the current in R860 with no resultant bright-up. Only when the B sweep is running also does R859 introduce a further -2mA to cause bright-up.

In the 'A Intensified by B' mode, with S702 operated, R851 and the Contrast control R850 defines a current between approximately 0.7mA and 2mA into the emitter of TR749 and hence through TR150. Thus during the A sweep the output current is between -0.6mA and -2mA (partial bright-up). When the B ramp is running also R859 introduces a further -2mA for full bright-up.

In the 'A and B Alternate' modes, with S704 selected, D730 energises the contrast path R850 and R851.

During the A display sweep, the circuit operates as for 'A Intensified by B' above. During the B display sweep the $\overline{Q}$ of IC708a will be low, turning off TR750. The current from TR749 flows through D723 but the output currents are as for 'B' only.

In X-Y, selected by S705, the A and B timebase signals are inhibited and R854 draws 4mA via D728, TR749 and TR750 for a resultant output of −2mA for a steady bright-up.

4.6.5 CALIBRATOR (Fig. 11)

This circuit provides a readily accessible calibration source for the 'Y' amplifier. Its output is provided at the front panel.

The circuit consists of an operational amplifier IC714 connected as a relaxation oscillator with R983 and C844 forming the feedback timing elements. The output voltage swing of IC714 gates a current, derived from the +12V line via R985, into the output resistors R987 and the close tolerance component R986. When the output of IC714 is low, diode D822 is biased on by the positive supply line and current flows into the op-amp output. When the amplifier outpu is high, D822 is biased off and D821 conducts, passing current into the output calibration resistors. C845 limits the maximum slew rate of the output edges. The output available for calibration purposes is 1.0V or 1mA into a shorting link between the output pin and ground connector.

DISPLAY MODE	CONDITION	TR 750 COLLECTOR CURRENT		'A' GATE CURRENT THRO' R860	'B' GATE CURRENT THRO' R859	NET CURRENT TO BRIGHT UP AMP VIA PT. 708	
		CONTRAST MIN	CONTRAST MAX			CONTRAST MIN	CONTRAST MAX
'A'ONLY	WAITING	−2mA	−2mA	0	0	0	0
	RUNNING	−2mA	−2mA	−2mA	0	−2mA	−2mA
'B' ONLY	'A' & 'B' WAITING	0	0	0	0	+2mA	+2mA
	'A' RUNNING 'B' WAITING	0	0	−2mA	0	0	0
	'B' RUNNING	0	0	−2mA	−2mA	−2mA	−2mA
A INTENS BY B	'A' & 'B' WAITING	−2mA	−0.6mA	0	0	0	+1.4mA
	'A' RUNNING	−2mA	−0.6mA	−2mA	0	−2	−0.6mA
	'A' & 'B' RUNNING	−2mA	−0.6mA	−2mA	−2mA	−4mA	−2.6mA
A & B ALT.	'A' & 'B' WAITING	−2mA or 0	−0.6ma or 0	0	0	0 or +2mA	+1.4 or +2mA
	'A' RUNNING	−2ma	−0.6mA	−2mA	0	−2mA	−0.6mA
	'B' RUNNING	0	0	−2mA	−2mA	−2mA	−2mA
X-Y		−4mA	−4mA	0	0	−2mA	−2mA

Chart of Display Currents Control for The Bright Up Amplifier

4.7 OPERATION WITH DM3010

This section covers the control circuitry of the OS3500 which operates specifically with the DM3010. The full circuit description of the DM3010 is included in the handbook for that unit and reference should be made to that also for a full understanding of the complete system.

4.7.1 TIME AND 1/TIME MEASUREMENT (Fig. 9)

In this mode of operation, the timebase system has to generate B sweeps at two positions on the A sweep. The first occurs at the time set by the normal DELAY control of the OS3500. The second is delayed with respect to the first by a period set by the v/t control of the DM3010. This section should be read in conjunction with Section 4.4.4 and 4.4.5 describing the independent operation of the dual timebase system.

At the end of each A sweep, the emitter of TR703 goes positive and this transistion is coupled through D711, R731 and C763 to produce a positive 'spike' at the input to IC707c. This gate inverts the impulse to apply a clock signal to bistable IC705b. This bistable is normally held in the preset state with 0V applied to SKU pin 7. This is applied via a shorting link on SKU if a DM3010 is not fitted and via switch contacts of DM3010 if fitted. When Time or 1/Time modes are selected by DM3010, this link is broken and IC705b is free to switch state at the end of each A ramp. The Q and $\overline{Q}$ outputs thus enable either comparator IC710a or comparator IC710b on alternate A sweeps. IC710a follows the normal DELAY setting while IC710b follows the additional delay level from the DM3010 via SKU pin 5. (See Section 4.1.7).

When the Y display mode 'CH1 and CH2 Alternate' mode is selected, R906 is connected to 0V by S711, and TR747 is free to switch under control of the signal from the beam switch bistable via SKT pin 18. The collector output of TR747 is applied to the K input of IC705b. Both bistables are clocked at the end of the A sweep and this link keeps them in step so that the normal Delayed B sweep is applied to CH1 displaying sweeps and the additionally delayed B sweep to CH2.

When Time Measurement and Trigger View are selected together, four different trace modes are required in sequence. The order is as follows:

Trig View/1st Time Delay,
Trig View/2nd Time Delay,
CHOP Y1 & Y2/1st Time Delay,
CHOP Y1 & Y2/2nd Time Delay.

As can be seen from the above, the Y/Trigger View channel switch bistable state must be changed on only every other timebase sweep. If 'CHOP' Mode is selected, pin 2 of IC707a rises high. If TRIGGER VIEW is selected, pin 1 rises high because the -12V bias to R840 and D753 is removed. This enables the gate IC707a IC707a to pass the switching signal from IC705b to the gate IC707b pin 3, and so produce half rate Alternate pulses at IC707b pin 6. However, if either of the modes 'A & B ALT' of 'COMP TRIG' are selected, pin 1 of IC707a is brought low again, and the gate does not pass this signal. If ' A & B ALT' is selected, -12V is applied from S704 to D752 to provide pull down current via R840 with D753 acting as a clamp. If 'COMP TRIG' is selected, pin 1 of IC707a is grounded by S508 on the Trigger Source switch assembly. The purpose of these two inhibit modes is to prevent the number of traces reaching 12 if ' A & B ALT' is selected and to inhibit the TRIG VIEW function when 'COMP TRIG' is selected.

For other Y channel modes, e.g. when 'CH1/CH2 ALT' and 'A & B ALT' is selected, the Internal (1st Delay) time measurement sweep is displayed on CH1 and the V/T controlled Delay (2nd Delay) on CH2, accomplished by phasing the bistable IC705b as described previously. The sequence is then A CH1 (1st Delay), A CH2 (2nd Delay), B CH1 (1st Delay) and B CH2 (2nd Delay); where A & B refer to the A and B sweeps. It is therefore apparent that only 4 traces are displayed and the sequencing of CH1/CH2 follows with Delay L/Delay 2, so no division of the Alternate pulse is necessary.

4.7.2 VOLTAGE MEASUREMENT (Fig. 9)

The generation of the additional Y shift signal which is applied to the CH2 channel when the DM3010 is set to Voltage measurement via the OS3500 is described in Section 4.4.2. Control of this offset switching is derived from IC705a.

This bistable is normally inhibited from responding to 'end of A sweep' clock signals by a high applied to its preset input via SKU pin 7. This is maintained by a shorting link when no DM3010 is fitted and via the relevant switch on the DM3010 if fitted. However, when this contact is broken, IC705a is free to respond to its clock inputs and its Q and $\overline{Q}$ outputs levels reverse state on alternate A sweeps, controlling the Y shift generator of CH2 via SKT pins 1 and 3.

The Q output of this bistable also controls gate IC707b to inhibit every other 'alternate' switching signal to the Y channel beam switch. Thus when 'CH1 and CH2 Alternate' mode of Y display and DM3010 voltage measurement are selected the sweep sequence will be CH1, CH2/normal shift, CH2/additional shift, presenting a 3 trace display.

The simultaneous application of 'A and B Alternate' timebase mode with DM3010 voltage measurement is inhibited. Warning of this prohibited combination is given as the relevant l.c.d. on the DM3010 is energised from the −12V supply via S704 and R911. This same signal line applies preset to IC705a to inhibit the voltage measurement sequence. A similar inhibit is applied to IC705a via S705, R841 and D754 when X-Y display mode is selected and voltage measurement does not apply.

5.1 GENERAL

The instrument is protected electrically by 2 fuses.

1) FS1 in the line of the incoming supply. This is a 20 x 5mm slow blow type. 500mA rating is required for the 220V/240V ranges or 1A rating for the 100/120V ranges. (Part No. 33685 or 34790).
2) A 20 x 5mm 500mA slow blow fuse in the +75/+150V supply mounted on the power supply p.c.b. (Part No. 33685).

The following sections give information on obtaining access to all internal front controls and removal of the various printed circuit boards and assemblies as may be found necessary, during fault finding.

If, during fault finding, a component needs replacing, it is recommended that it is cut from the printed circuit board as close as possible to the component, leaving the wires connected to the copper track and protruding through to the component side of the board. The new component should then be soldered into position by attaching it to these protruding wires. This protects the copper track from damage.

If a fault on a printed board cannot be cleared it is recommended that the instrument is returned to the manufacturer for repair. When faults have been cleared it is advisable for the calibration procedure to be implemented to ensure that the instrument conforms to the specification. Note that all knobs on the front panel have collet fixing. They are removed by prising out the central cap, slackening the fixing screw and then withdrawing the knob from the shaft. The outer knob of a co-axial control has a nut fixing, not a screw.

5.2 ACCESS

Immediate access is available to nearly all preset controls once the top and bottom covers have been removed.

Figures 13, 14 & 15 illustrate various views of the instrument showing the position of these presets and the major sub-assemblies of the instrument. Each cover is retained in position by four latch fasteners. Each fastener is released by turning it one quarter of a turn clockwise or counterclockwise. In the locked position the arrow head on the fastener points toward the adjacent frame.

WARNING: The instrument should be disconnected from the supply while the covers are being removed. Dangerous high voltages are then accessible and the instrument should be operated only by suitably qualified personnel.

The following description details the method for removing the individual assemblies.

5.2.1 ATTENUATOR & PRE-AMPLIFIER ASSEMBLY

1. Remove the knobs from the Y attenuator switches and Y shift controls.
2. Remove the two nuts holding the attenuator switches to the front panel.
3. Unplug the multiway connector (SKT or SKM) from the timebase to the Y-amplifier at the timebase end.
4. Unclip the Delay Line cable from its fixings around the tube shield, and check the cable routing to ensure that there is sufficient slack available to withdraw the Y-preamplifier.
5. Remove the 3 way plug from the socket SKN at the rear of the Y-preamplifier p.c.b.
6. Remove the retaining screws (4 per side) securing the LHS and RHS preamplifier front screens. This exposes the three way plugs which connect to the 'UNCAL' leads which should also be unplugged.
7. The Y-preamplifier p.c.b. is retained by 5 fixing screws. The p.c.b. is mounted on the LHS sidebar by two pillars and on its RHS by 3 small blocks which are also screwed to the timebase. Firstly, remove the screws holding the board to the sidebar pillars. Then slacken the screw retaining the front pillar to the sidebar so that the front pillar can be moved back towards the rear pillar. Note that the screw retaining the p.c.b. at the rear pillar is a nylon type. Next, remove the remaining 3 screws retaining the board to the timebase mounting blocks. The Y-preamplifier can the be withdrawn by sliding the assembly outwards and backwards, ensuring that the CH2 attenuator cover does not foul on the front fixing of the timebase mounting block as this is done. Note that it is necessary to unsolder the PTFE co-axial leads if complete removal of the assembly is required.

5.2.2 Y OUTPUT ASSEMBLY

1. Remove the following plugs from their sockets on the p.c.b.:-
   SKG (2 way lockable) to power on LED
   SKH (4 way) EHT INPUT
   SKJ (2 way lockable) to scale lamps
   SKK (2 way) trace rotate (see note)
   SKL (11 way) power input

   NOTE: SKK is reversible and it is useful to mark its polarity before removal. The lockable sockets SKG, SKJ and SKK are retained by a small flap which should be bent back for easy removal of the plug.
2. Unclip the Delay Line from the c.r.t. and allow sufficient slack line for removal of the p.c.b. Note that for complete withdrawal of the Y output assembly the Delay Line must be unsoldered from pins 400(0V), 401 and 402 of the p.c.b. It will be necessary to mark the Delay Line connections to ease recognition for reassembly.
3. Remove the knobs from the INTENSITY, FOCUS and SCALE controls.
4. Remove the two Y deflection plugs and the Geometry connection from the c.r.t.

5. Remove the sidebar trim by inserting a screwdriver in the slot near the front panel, and then prising the trim away from the sidebar.
7. Remove the screw attaching the transistor heat sink to the sidebar, and the two board fixing screws.
8. Remove the top support bar. The assembly may now be withdrawn to the length of the Delay Line.

5.2.3 TRIGGER UNIT

1. Remove the knobs from the $\overline{A}$ level, $\overline{B}$ level and $\overline{A}$ Hold Off controls.
2. Unsolder the two leads connecting to the A Trigger l.e.d. (D15) at points 509, 510 on trigger p.c.b. (Black wire to 510, Red wire to 509).
3. Unsolder the input connections from the EXT A and EXT B sockets to the EXT X attenuator p.c.b. Then unscrew the two screws retaining the board mounting pillars to the front panel.
4. Remove the small screen between the trigger assembly and timebase assembly which is held in place by the single screw on the rear left corner of the trigger switch p.c.b.
5. Remove the two screws on the trigger p.c.b. which hold the board to the connecting pillars mounted on the timebase p.c.b. (One screw is on the rear of the board, the other is just in front of the B LEVEL control potentiometer).
6. Remove the plugs from SKR and SKP and unscrew the 'P' clip from the timebase p.c.b., which retains the co-axial cables connecting between the trigger assembly and the timebase.
7. Remove the remaining two screws which support the trigger p.c.b. brackets to the main side bar on the right hand side of the instrument. The trigger assembly may now be removed by sliding the unit backwards sufficiently to clear the control potentiometer shafts and switch buttons. Then tilt the front of the unit downwards and withdraw it from the instrument. If it becomes necessary to remove the co-axial leads these should first be marked. They may be withdrawn by unsoldering the inner from the 'V' shaped connector and then melting the solder on the outer connector and withdrawing the cable.
   NOTE that when the screws are removed holding the trigger p.c.b. supports to the side frame, the captive nuts may slide along the channel and will need to be re-positioned.

5.2.4. TIMEBASE UNIT

Removal ot the timebase p.c.b. is most easily accomplished by firstly removing the trigger assembly as described above.

1. After withdrawing the trigger assembly, unsolder the 'A' trigger output and 'B' trigger output leads from the trigger board at points 511, 512 and 554, 555 respectively.
2. Unsolder the calibrator output from the rear of the timebase p.c.b. at points 711, 712. (The A ramp output and B gate output leads are reasonably long and may be left connected).
3. Remove the connections from the timebase board to the X plates on the c.r.t. (The pink wire connects to the c.r.t. pin nearest the timebase board and the brown wire to the next pin for reference).
4. Unscrew the solder tag from the chassis to the copper side of timebase board, adjacent to the X plate leads.
5. Remove the plugs from sockets SKW (power input) SKX (B timebase controls) SKV (A timebase controls) SKT (Y-amplifier interconnection).
6. Unscrew the 3 screws retaining the timebase to the Y-amplifier p.c.b. One is just behind the 'ALT' switch, S711, the second is just to the left of SKS and the third is to the right of SKT. Next, remove the 3 screws retaining the timebase to the top rail.
7. The timebase board may now be removed by sliding the unit backwards to clear the switch push buttons and then downwards at the rear end and out via the bottom of the instrument, being careful not to catch the heatsinks of the X output amplifier transistors on the transformer.

5.2.5 E.H.T. UNIT

1. Remove the p.d.a. cavity cap connector from the front of the c.r.t. and carefully discharge the multiplier by shorting the connector to chassis. Also short the c.r.t. p.d.a. connection to chassis using a long shafted screwdriver with an insulated handle.
2. Remove the top screen of the unit by unscrewing the three retaining screws.
3. Remove the plug from SKE on the e.h.t. board.
4. The e.h.t. multiplier and p.c.b. may now be extracted from the instrument by removing the two screws retaining the multiplier and the four screws retaining the Oscillator p.c.b. Note that when refitting the top cover the two captive nuts on the side bar must be adjusted to the correct positions.

5.2.6 POWER SUPPLY ASSEMBLY

The main power supply is a removable assembly forming the rear of the instrument. Removal of the power supply board is most easily accomplished by first detaching the assembly from the instrument.

1. Remove the four screws on the inside rear of the instrument which are nearest to the corners. This will release the rear mounting feet, and expose the four countersunk screws which retain the unit to the side frames.
2. Remove rear cover plastic moulding held by the four retaining screws.
3. Unsolder the co-axial leads from the A RAMP and B GATE output BNC sockets on the rear panel and mark the leads for identification.

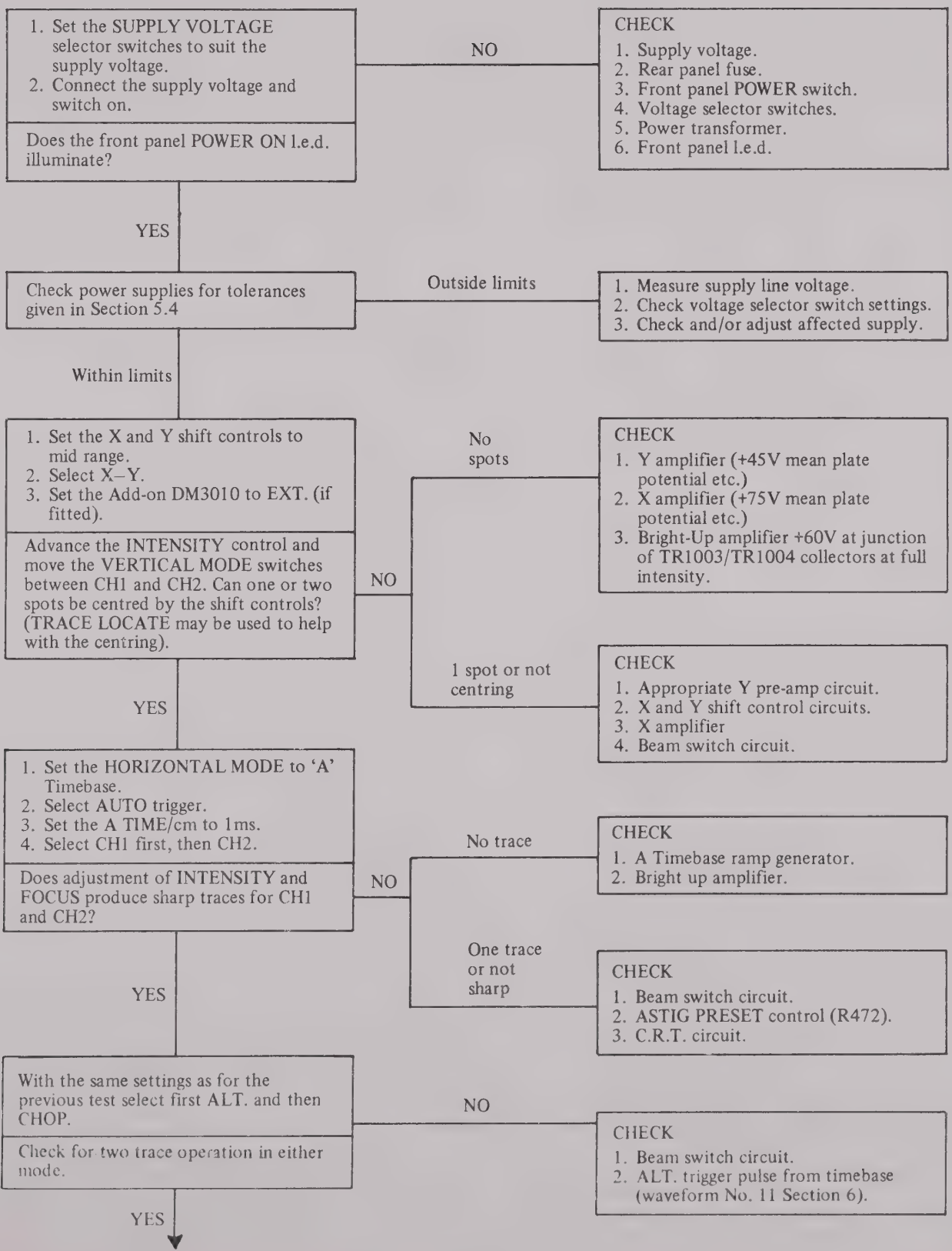
4. Unsolder the green and brown twisted pair from the transformer tags (marked 0 & 0.3V on the center pins of the secondary windings).
5. Unsolder and mark for identification the two screened leads CHOP BLANK and BLANK from the power supply p.c.b. on pins 1014/0V and 1013/0V, respectively. Also remove the plugs from SKA(CRT), B, C, D, and the mechanical connection to the power ON/OFF switch.
6. Remove the four countersunk screws holding the unit to the side frames and the two countersunk screws retaining it to the top bars. Then withdraw the Unit.

5.2.7 CATHODE RAY TUBE

1. Remove and discharge the p.d.a. connector in the manner described in Section 5.2.5, item 1.
2. Unclip the delay line from the four mounting clips positioned around the tube shield.
3. Remove the rear panel plastic cover held by four retaining screws.
4. Remove the c.r.t. base connector, and the trace rotate connection plug from SKK on the Y output amplifier board.
5. Remove the c.r.t. side pin connections.
6. Remove the two screws retaining the c.r.t. shield at its rear to the e.h.t. mounting bracket.
7. Slide the tube and shield backwards sufficiently to clear the tube support moulding at the front of the instrument until it can be lifted out.
8. The tube may now be released from its shield by releasing the locking clamp at the rear of the tube shield and sliding the tube forward. Care should be taken not to bend the tube side pins when doing this. Note that the leads to the trace rotation coil on the c.r.t. pass through a grommeted hole in the tube shield. The inserts of the connecting plug on these leads should be withdrawn from the housing to allow clearance through this hole.
9. When replacing the c.r.t. assembly, the reverse procedure should be followed but the locking clamp should be tightened last, after pushing the tube forward within the shield to meet the front panel. DO NOT overtighten this clamp as the glass may be damaged. Tighten only to the point where the rubber block is seen to distort.

5.3 FAULT FINDING TABLES

Fault finding is based initially on the characteristics of the fault and the tables of Section 5.3 define a suggested procedure to localise the fault to one particular area. Subsequent detailed guidance will be obtained from the relevant circuit diagram and circuit description and from the table of operating potential in Section 5.4.


1. Set the SUPPLY VOLTAGE selector switches to suit the supply voltage.
2. Connect the supply voltage and switch on.
Does the front panel POWER ON l.e.d. illuminate?
NO
CHECK
1. Supply voltage.
2. Rear panel fuse.
3. Front panel POWER switch.
4. Voltage selector switches.
5. Power transformer.
6. Front panel l.e.d.
YES
Check power supplies for tolerances given in Section 5.4
Outside limits
1. Measure supply line voltage.
2. Check voltage selector switch settings.
3. Check and/or adjust affected supply.
Within limits
1. Set the X and Y shift controls to mid range.
2. Select X–Y.
3. Set the Add-on DM3010 to EXT. (if fitted).
Advance the INTENSITY control and move the VERTICAL MODE switches between CH1 and CH2. Can one or two spots be centred by the shift controls? (TRACE LOCATE may be used to help with the centring).
NO
No spots
CHECK
1. Y amplifier (+45V mean plate potential etc.)
2. X amplifier (+75V mean plate potential etc.)
3. Bright-Up amplifier +60V at junction of TR1003/TR1004 collectors at full intensity.
1 spot or not centring
CHECK
1. Appropriate Y pre-amp circuit.
2. X and Y shift control circuits.
3. X amplifier
4. Beam switch circuit.
YES
1. Set the HORIZONTAL MODE to 'A' Timebase.
2. Select AUTO trigger.
3. Set the A TIME/cm to 1ms.
4. Select CH1 first, then CH2.
Does adjustment of INTENSITY and FOCUS produce sharp traces for CH1 and CH2?
NO
No trace
CHECK
1. A Timebase ramp generator.
2. Bright up amplifier.
One trace or not sharp
CHECK
1. Beam switch circuit.
2. ASTIG PRESET control (R472).
3. C.R.T. circuit.
YES
With the same settings as for the previous test select first ALT. and then CHOP.
Check for two trace operation in either mode.
NO
CHECK
1. Beam switch circuit.
2. ALT. trigger pulse from timebase (waveform No. 11 Section 6).
YES

1. Set the VOLT/cm switches to 0.2V.
2. Set the VOLT/cm VARIABLE to CAL.
3. A TIME/cm to 0.5ms.
4. Set TIME/cm VARIABLE to CAL.
5. Select DC TRIG & +ve slope.
6. Select CH1 or CH2 as trigger source.
7. Select AUTO mode.

Inject a 1V CAL waveform into CH1 or CH2 (as selected by stage 6), and adjust the TRIG LEVEL for a stable trigger. Does it produce 1 cycle per two cms. and 5 cms amplitude on both channels?

NO

- Sweep speed error. (For accurate check use Time Mark Generator

  CHECK
  1. Timebase
  2. X amplifier
  3. Check calibrator.

- Not 5cm

  CHECK
  1. Appropriate Y channel circuit.
  2. Remaining Y amplifier circuits.
  3. Check calibrator.

- Not triggering

  CHECK
  1. Appropriate Y trigger pick off amplifier.
  2. Trigger source switch and wiring.
  3. A Trigger amplifier.
  4. A Timebase bistable (IC701b) and associated circuitry.

YES

Set as for the previous check except:-
1. Set A TIME/cm to 5ms.
2. Set X Amp PULL X10.

Check for 1 cycle/two cms.

NO

CHECK
1. Pull X10 switch & wiring.
2. X amplifier

YES

1. Return the PULL X10 switch to the X1 position.
2. Set the B trigger level control to the 'B STARTS AFTER DELAY' position.
3. Select 'A INTENS BY B'.
4. Set the B TIME/cm to 0.5ms.

Check for a brightened up portion on the display.

NO

CHECK
1. Contrast preset R850 adjustment on timebase.
2. C.R.T. grid bias adjustment R1119 (E.H.T. UNIT).
3. B Timebase.
4. Combining gate circuitry (TR749, TR750) on timebase for Bright up amplifier.
5. Check Bright up output shows a +ve step during the B sweep time.
6. Delay pick off comparator (IC710b).
7. Check that shorting plug is fitted on SKU or, if DM3010 is fitted that pin 6 of SKU is low.
8. Bistable IC705b.
9. Gating circuitry, IC703.

YES

Rotate the DELAY control.

Check that brightened up portion moves.

NO

CHECK
1. Delay potentiometer.
2. Buffer amplifier (IC706).
3. Delay comparator (IC710b).

YES

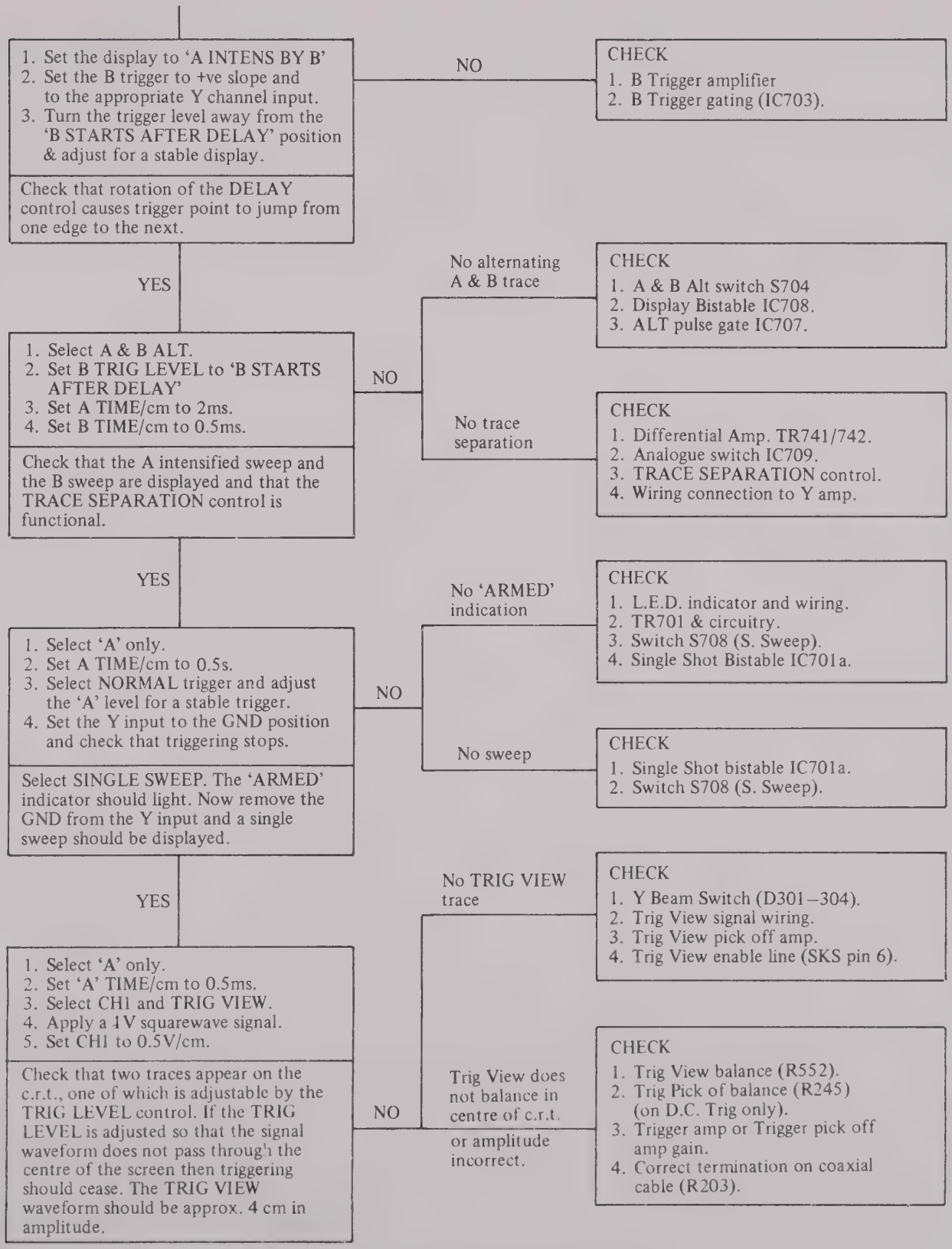
1. Set the display to 'B'.

Check for 1 cycle/2cms.

NO

CHECK
1. B Timebase calibration.

YES


1. Set the display to 'A INTENS BY B'
2. Set the B trigger to +ve slope and to the appropriate Y channel input.
3. Turn the trigger level away from the 'B STARTS AFTER DELAY' position & adjust for a stable display.
Check that rotation of the DELAY control causes trigger point to jump from one edge to the next.
NO
CHECK
1. B Trigger amplifier
2. B Trigger gating (IC703).
YES
1. Select A & B ALT.
2. Set B TRIG LEVEL to 'B STARTS AFTER DELAY'
3. Set A TIME/cm to 2ms.
4. Set B TIME/cm to 0.5ms.
Check that the A intensified sweep and the B sweep are displayed and that the TRACE SEPARATION control is functional.
NO
No alternating A & B trace
CHECK
1. A & B Alt switch S704
2. Display Bistable IC708.
3. ALT pulse gate IC707.
No trace separation
CHECK
1. Differential Amp. TR741/742.
2. Analogue switch IC709.
3. TRACE SEPARATION control.
4. Wiring connection to Y amp.
YES
1. Select 'A' only.
2. Set A TIME/cm to 0.5s.
3. Select NORMAL trigger and adjust the 'A' level for a stable trigger.
4. Set the Y input to the GND position and check that triggering stops.
Select SINGLE SWEEP. The 'ARMED' indicator should light. Now remove the GND from the Y input and a single sweep should be displayed.
NO
No 'ARMED' indication
CHECK
1. L.E.D. indicator and wiring.
2. TR701 & circuitry.
3. Switch S708 (S. Sweep).
4. Single Shot Bistable IC701a.
No sweep
CHECK
1. Single Shot bistable IC701a.
2. Switch S708 (S. Sweep).
YES
1. Select 'A' only.
2. Set 'A' TIME/cm to 0.5ms.
3. Select CH1 and TRIG VIEW.
4. Apply a 1V squarewave signal.
5. Set CH1 to 0.5V/cm.
Check that two traces appear on the c.r.t., one of which is adjustable by the TRIG LEVEL control. If the TRIG LEVEL is adjusted so that the signal waveform does not pass through the centre of the screen then triggering should cease. The TRIG VIEW waveform should be approx. 4 cm in amplitude.
NO
No TRIG VIEW trace
CHECK
1. Y Beam Switch (D301–304).
2. Trig View signal wiring.
3. Trig View pick off amp.
4. Trig View enable line (SKS pin 6).
Trig View does not balance in centre of c.r.t.
or amplitude incorrect.
CHECK
1. Trig View balance (R552).
2. Trig Pick of balance (R245) (on D.C. Trig only).
3. Trigger amp or Trigger pick off amp gain.
4. Correct termination on coaxial cable (R203).

FOR INSTRUMENTS FITTED WITH DM3010

1. Select time measurement.
2. Select 'A INTENS BY B'
3. Set DM3010 V/T control to maximum.
4. Select CH1 or CH2.

Check that for each 'A' timebase range the DM3010 reads the correct FSD, with the correct time notation (i.e. s, ms, μs) and decimal point.
e.g. 50ns/cm should read 0.5μs FSD.

NO

CHECK
1. A TIME/cm switch.
2. Wiring harness to DM3010.
3. DM3010 Logic.
4. DM3010 calibration.
5. V/T control.

YES

1. Set the A TIME/cm to 20μs.
2. Set the B TIME/cm to 1μs.
3. Apply 10μs markers.
4. Set the DELAY control to the minimum value which aligns the 1st Bright up with the first available marker.
5. Set the V/T control to maximum.

Check that two Bright ups occur on the display 10 cm apart and that the final Bright up corresponds with the 20th marker.

NO

Only one Bright up

CHECK
1. Delay comparator (IC710).
2. Bistable IC705b.
3. Wiring harness to SKU.
4. DM3010 time switches (S8 & S9).

Both Bright ups will not align with markers

CHECK
1. A Timebase calibration.
2. DM3010 V/T control calibration.
3. Delay comparators (Ic710 a & b).

YES

1. With the settings as for the previous check except select 'B' only.

Check that the marker from first Delay sweep aligns with the marker from the second Delay sweep within the calibration specification.

NO

CHECK
1. A Timebase calibration.
2. DM3010 V/T control calibration.

YES

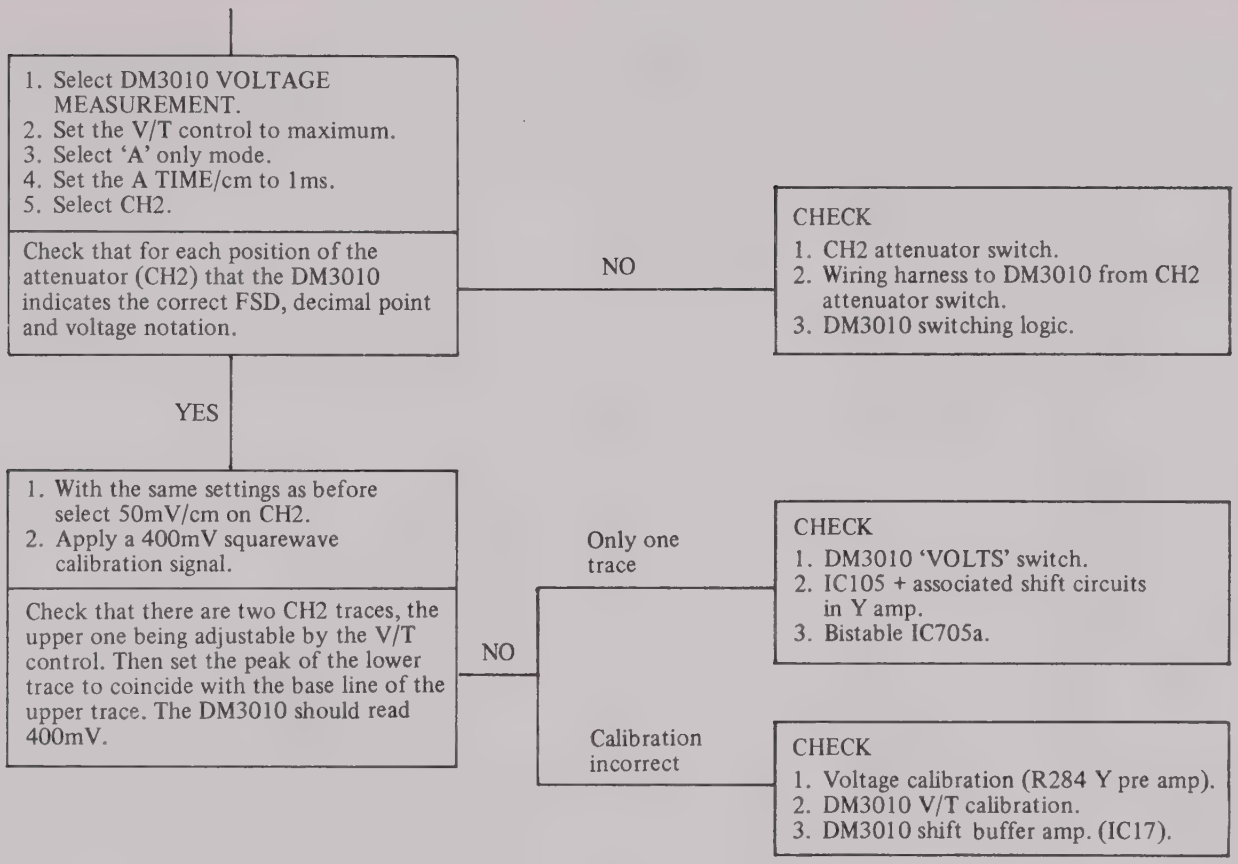
1. Using the same setting as for the previous check except select CH1 & CH2 ALT.

Check that the first Bright up occurs on CH1 and the second on CH2 and that the 'B' traces correspond to the respective channels.

NO

CHECK
1. Bistable IC705b.
2. Channel switch phasing (Pin 18 SKT to TR747).
3. Display bistables IC708a & IC708b.
4. Gate IC707.

YES


1. Select DM3010 VOLTAGE MEASUREMENT.
2. Set the V/T control to maximum.
3. Select 'A' only mode.
4. Set the A TIME/cm to 1ms.
5. Select CH2.
Check that for each position of the attenuator (CH2) that the DM3010 indicates the correct FSD, decimal point and voltage notation.
NO
CHECK
1. CH2 attenuator switch.
2. Wiring harness to DM3010 from CH2 attenuator switch.
3. DM3010 switching logic.
YES
1. With the same settings as before select 50mV/cm on CH2.
2. Apply a 400mV squarewave calibration signal.
Check that there are two CH2 traces, the upper one being adjustable by the V/T control. Then set the peak of the lower trace to coincide with the base line of the upper trace. The DM3010 should read 400mV.
NO
Only one trace
CHECK
1. DM3010 'VOLTS' switch.
2. IC105 + associated shift circuits in Y amp.
3. Bistable IC705a.
Calibration incorrect
CHECK
1. Voltage calibration (R284 Y pre amp).
2. DM3010 V/T calibration.
3. DM3010 shift buffer amp. (IC17).

5.4 OPERATING POTENTIALS

Unless otherwise stated it is assumed that the power supply input voltage is approximately at the mid-range of the Supply Voltage setting. The power supply voltages in the tables are those appearing under these conditions. Other voltages assume that the Y inputs are grounded and the amplifiers are set to 2mV/cm sensitivity. The Timebase is set to AUTO with the trigger level control fully clockwise, and the Y amplifier to CH1 mode with CH1 trace brought to the center of the screen or CH2 mode with CH2 trace brought to the center of the screen for the relevant channel operating potentials.

Y PRE AMPLIFIER

LOCATION		
TR105	BASE	APPROX -8V (DEPENDENT ON TR101 TOLERANCES)
TR103	EMITTER	0V
TR107 and TR109	COLLECTORS	+2.4V
TR111 and TR113	COLLECTORS	-5.0V
TR119 and TR121	COLLECTORS	-3.7V
TR123 and TR125	EMITTERS	-2.3V
TR127 and TR129	EMITTERS	-6.5V
IC301 PIN 13		+2.6V (+4.1V CH2 selected)
IC302 PIN 13		+4.1V (+2.6V CH2 selected)
TR303 and TR304	EMITTERS	+6.6V
PINS 151 & 152	DELAY LINE INPUT	+1.2V

Voltages for channel 2 selected in NORMAL (non-voltage measurement) mode if 3010 fitted.

TR128 and TR130	COLLECTORS	-1.9V
TR133	COLLECTOR	-2.6V

Y OUTPUT AMPLIFIER

LOCATION		
TR400 and TR401	COLLECTORS	-4.2V
TR406 and TR407	BASES	+3.5V
TR408 and TR409	BASES	+3.1V
TR411 and TR412	COLLECTORS	+43V

TRIGGER AMPLIFIER

These readings are taken with the TRIGGER LEVEL controls (A & B) set to mid-position, and no trigger signal applied.

A CHANNEL

LOCATION		
TR503	BASE	0V
TR507	BASE	-0.74V
TR508	BASE	-0.97V
TR507/TR508	COLLECTORS	+3.0V
TR506	EMITTER	+4.0V (X-Y not selected) +2.0V (X-Y selected)
TR509/TR510	COLLECTORS	-0.9V
TR513/TR514	COLLECTORS	+3.9V
IC501	PIN 5	3.8V (NORMAL TRIG) 4.5V (INVERT TRIG)
IC501	PIN 10	+2.1V (NORMAL TRIG) 3.8V (INVERT TRIG)
TR515	EMITTER	-4.7V
TR517	EMITTER	-11.7V
TR511/TR512	COLLECTORS	+5.5V (TRIG VIEW selected)

B CHANNEL

TR522	BASE	0V
TR524	BASE	-0.74V
TR525	BASE	-0.97V
TR524/TR525	COLLECTORS	+3.0V
TR526/TR527	COLLECTORS	-0.9V
TR528/TR529	COLLECTORS	+3.8V
IC502	PIN 5	+4.5V (NORMAL TRIG) +3.8V (INVERT TRIG)
IC502	PIN 10	+3.8V (NORMAL TRIG) +2.1V (INVERT TRIG)

TIMEBASE

Readings are taken with the A ONLY and NORMAL TRIG modes selected. No trigger signal should be applied. All controls to be in the CAL position unless otherwise stated.

TR714	BASE	+14.5V
TR738	BASE	+14.5V
TR714	BASE	+21V †
TR738	BASE	+21V †

† A & B VARIABLE TIME/CM fully A/clockwise

TR720	EMITTER	0V
TR710	EMITTER	-8.6V
TR703	EMITTER	+3.0V
TR735	EMITTER	0V
TR727	EMITTER	-8.6V
TR726	EMITTER	+3.0V
TR749	BASE	-2.2V
TR750	COLLECTOR	+3.0V

X OUTPUT AMPLIFIER

LOCATION		
TR814	EMITTER	

These readings taken with the timebase set to the X-Y mode, the A TRIGGER SOURCE to EXT and the X shift adjusted for a spot in the center of the c.r.t.

LOCATION		
TR810/TR812	BASES	+2.0V
TR809/TR811	BASES	+2.0V
TR813	EMITTER	+8.0V
TR805	BASE	+6.9V
TR806	BASE	+7.5V
TR807	BASE	+8.2V
TR808	BASE	+7.5V
TR801 and TR803 TR802 and TR804	COLLECTORS	+75V

TIMEBASE WAVEFORMS (Figs. 2 & 3)
These are drawn for the following conditions. The 'A' timebase is switched to 0.1ms/cm and the 'B' timebase to 10μs/cm. A 5cm 10kHz square wave is applied to the CH1 channel, and the 'A' trigger set to CH1 +ve slope. The 'B' trigger is set to B STARTS AFTER DELAY, or to CH1 +ve slope. The delay multiplier potentiometer is set to about 5.

5.5 CALIBRATION PROCEDURE

5.5.1 TEST EQUIPMENT

1. Variable autotransformer (Variac). Output voltage 95 to 260V at 1A with ac rms Voltmeter.
2. Digital multimeter 3½ digit, with 1 Megohm minimum input impedance and an accuracy within 0.2%.
3. High voltage probe for multimeter capable of operation up to 20kV.
4. Voltage Calibrator. 1kHz square wave generator with amplitude 2mV to 50V. Accuracy within 0.2%.
5. Time Mark Generator. Marker generator of 10ns to 0.5 sec. Accuracy within 0.2%.
6. Squarewave Generator. 100Hz – 1MHz flat top square wave generator with adjustable amplitude 0.1V to 1V into 50 ohms having a rise time of less than 1ns.
7. R.F. Sinewave generator. 500kHz to 100MHz with 50kHz reference frequency. Output amplitude 10mV to 5V p-p into 50 ohms. Amplitude accuracy at 50kHz and 500kHz to 60MHz within 3%.
8. LF Sinewave Generator.
9. Capacitance Standardiser. 1mΩ/28pF, BNC 50Ω termination, BNC-BNC connector lead (PL43).
10. Test Oscilloscope, 10MHz bandwidth, $\geqslant$5% accuracy $\leqslant$50mV/cm sensitivity with x10 low capacitance probe.

NOTE. Calibration should be carried out at normal ambient temperature and should not be commenced until the instrument has been operating for at least 15 mins.

5.5.2 POWER SUPPLIES AND CALIBRATOR

1. Set the INTENSITY control to minimum.
2. Set the SUPPLY VOLTAGE switches on the rear panel to suit the supply. Apply the supply voltage via the Variac set to mid-range of the supply voltage setting.
3. Check that the SCALE control varies the scale intensity and that the POWER on l.e.d. is energized.
4. Connect the digital voltmeter between chassis and Pin 5 on PLD (rear panel p.c.b.). Set R1052 to give -12.00 volt.
5. Apply the digital voltmeter to PLD on the following positions and check the supply voltages:–

PLD PIN NO.	NOMINAL VOLTAGE
8	5.0V ± 5%
3	24.0V ± 5%
1	162.0V ± 6%

6. Apply the digital voltmeter to orange lead (+ve) connection on C1 (1000μF 100V) and check for 75V ± 6%.
7. Briefly switch off the instrument, remove IC714 on the timebase board and then switch on again. Connect the digital meter between the 1V CAL pin and chassis. Adjust R1051 on the rear panel board for a +1.000V DC output. Now connect the digital meter to pin 6 of PLD and check for +12V supply ± 2%. Briefly switch off the set to return IC714 in place and switch on again. Confirm with a test oscilloscope the presence of a square wave at approximately 1kHx at the CAL output.

5.5.3 SET E.H.T. VOLTAGE AND TUBE CUT OFF

1. Remove the screen from the e.h.t. oscillator, held in place by the three retaining screws.
2. Connect the digital multimeter via the high voltage probe between chassis and the cathode (positive band) of D1114. Adjust R1106 for 1500V.
   BEWARE HIGH VOLTAGE.
3. Check the p.d.a. voltage at the front of the tube for +10.5kV ± 5%.
   BEWARE HIGH VOLTAGE.
4. Set the instrument to X–Y mode and centre the spot to be within the graticule area. Adjust the INTENSITY control for +15V (approx.) at R1022 (47kΩ) and then adjust R1119 for a spot which is just visible.
5. Replace the e.h.t. screen; first relocating the captive nuts on the side bar of the instrument.

5.5.4 TRACE ALIGNMENT, GEOMETRY & ASTIG

1. Set the instrument to 1ms/cm, 50mV/cm, with trigger on AUTO, timebase to 'A' only and CH1 mode selected.
2. Ground CH1 input and adjust the front panel control TRACE ROTATE (R467) for a horizontal trace. It may be necessary to reverse the plug connecting to SK–K to do this. (This is mounted on the Y output board on the left side of the instrument).
3. Set the CH1 input coupling to AC. Insert a 1kHZ sinewave signal at approximately 400mV amplitude. Adjust the trigger level control to trigger the waveform and adjust the FOCUS control and ASTIG preset control (R472) on the Y output p.c.b. for the finest trace at low INTENSITY setting.
4. Insert a 1MHz sinewave at approximately 400mV amplitude. Adjust the GEOMETRY preset control (R473) on the Y output p.c.b. for the best compromise flat horizontal and vertical edges at the extreme top, bottom and sides of the graticule.

Y AMPLIFIER ADJUSTMENTS

5.5.5 CHANNEL 1 & 2 AC/DC EQUALIZATION

1. Set CH1 VOLTS/cm switch to 10mV, INPUT COUPLING switch to DC, the VERTICAL MODE switch to CH1, A TRIGGER SOURCE to CH1, AC COUPLED. The Timebase should be set to A ONLY with the TIME/cm switch set to 5ms/cm.
2. Inset a 100Hz signal from the square wave generator to CH1 input and adjust R135 for a flat top square wave.
3. Repeat the procedure for R136 on CH2.

5.5.6 CHANNEL 1 & 2 DC STEP ATTENUATOR BALANCE

1. Set the CH1 VOLTS/cm switch to 2mV, INPUT COUPLING switch to GND, and allow the timebase to free run by selecting the AUTO function.
2. Set the Y shift to centre the trace on the screen and adjust R117 so that no trace movement occurs when the CH1 VOLTS/cm switch is turned to the 5mV position. Check also that no movement on the rest of the attenuator ranges.
3. Repeat the procedure for CH2 by adjustment of R118.

5.5.7 CHANNEL 1 & 2 FINE GAIN CONTROL BALANCE

1. Set the CH1 VOLTS/cm switch to 2mV, INPUT COUPLING to GND and allow the timebase to free run.
2. Adjust R151 such that operation of the CH1 FINE GAIN control does not produce significant trace movement.
3. Repeat the procedure for CH2 using R152.

5.5.8 CHANNEL 1 & 2 INVERT BALANCE

1. With CH1 input set as for step 1 on previous test press the CH1 INVERT switch, adjusting R231 so that no trace movement occurs between the normal and inverted input.
2. Repeat the procedure for CH2 using R232.

5.5.9 CHANNEL 1 & 2 ATTENUATOR COMPENSATION

1. Apply a 1kHz square wave from the Voltage Calibrator at an amplitude of 500mV to CH1 input.
2. Set CH1 INPUT COUPLING to DC, and the VOLTS/cm switch to 0.1V. Set the TIME/cm switch to 1ms.
3. Set C107 for a flat top on the square wave.
4. Apply a 1kHz 5V square wave signal from the Calibrator to CH1 input. Set CH1 VOLTS/cm to 1V.
5. Adjust C103 for a flat top square wave display.
6. Insert a 28pF capacitance standardiser between the calibrator output and the CH1 input. Apply a 10V signal from the calibrator and align C101 for a flat top square wave display.
7. Reduce the calibrator output to 1V and reset the CH1 VOLTS/cm switch to 0.1V. Then align C105 for a flat top signal.
8. Reduce the calibrator output to 100mV, set the CH1 VOLTS/cm switch to 10mV and align C109 for a flat top signal.
9. Repeat all the steps 1–8 for CH2, using the following trimmers:

Step 3 (0.1V compensation)	C108
Step 5 (1V compensation)	C104
Step 6 (Input capacitance 1V)	C102
Step 7 (Input capacitance 0.1V)	C106
Step 8 (Input capacitance 10mV)	C110

5.5.10 CHANNEL 1 & 2 GAIN CALIBRATION

1. Set R284 (DM3010 GAIN CALIBRATION) to mid-range, and the Y FINE GAIN controls

to the CAL position.
2. Apply a 1kHz 50mV square wave Calibrator signal to CH1 with the VOLTS/cm switch at 10mV and the input dc coupled. Adjust R22, for a 5cm peak to peak display.
3. Check that all VOLTS/cm ranges are accurate to within ±3%.
4. Repeat step 2 for CH2, adjusting R222 for a 5cm display.

5.5.11 Y–AMPLIFIER OVERALL PULSE RESPONSE

1. Initially set the trimmer and variable resistors as follows:–

	CH1	CH2	
Y PRE AMP P.C.B.	C127	C128	to mid-range
	C145	C128	Approx. 1/3 Capacitance

Y Output p.c.b.	C404	To mid range
	R414	To mid range
	C423	To minimum capacitance
	R446	To mid range

2. Apply a 100kHz signal at an amplitude of 50mV from the square wave fast edge generator to CH1. Set CH1 to 10mV/cm and INPUT COUPLING to DC. The Y FINE GAIN controls should be set in the CAL position. Set the TIME/cm to 5μs/cm.
3. Adjust C423 for an optimum square corner on the signal.
4. Apply a 1MHz signal from the generator at the same level and set the TIME/cm switch to 50ns/cm. Adjust R414 and C404 for approximately 20% undershoot over the first 20ns. (This facilitates the setting of step 5). Also adjust R145, if necessary, to achieve this.
5. Pull the X10 X expand switch on the X SHIFT control and set C422 and R446 for optimum square corner. A compromise adjustment between C127 on the preamplifier p.c.b. and the trimmers detailed in step 4 may be required to achieve this. The risetime on the leading edge should be below 6ns (typically about 5.2ns).
6. Transfer the generator input to CH2 and set the VOLTS/cm and COUPLING to the same conditions as for CH1. Select CH2 display mode.
7. Adjust C128 and C145 for the best square corner on the square wave signal. Note that it may be necessary to provide a compromise adjustment with CH1 trimmers, C127 and C145 together with the Y output trimmers C404, R414, C422 and R446 to achieve best performance and channel matching. Check that the leading edge risetime is below 6ns.

5.5.12 Y AMPLIFIER BANDWIDTH

1. Set CH1 and CH2 VOLTS/cm switches to 10mV, INPUT COUPLING to DC.
2. Select CH1 Mode and inject a 50kHz reference source from the Constant Amplitude Generator to give 5cm of deflection. Increase the Generator frequency until the displayed amplitude drops to 3.5cm. The frequency reading should be greater than 60MHz.
3. Repeat this procedure for the 50mV, 20mV, 5mV and 2mV positions of CH1 and for the 50mV, 20mV, 10mV, 5mV and 2mV ranges of CH2.

TIMEBASE ADJUSTMENTS

5.5.13 X MEAN PLATE VOLTAGE

1. Set the TIME/cm switch to 0.1ms/cm, the trigger mode to AUTO, and the HORIZONTAL MODE to 'A' only. Adjust the A TRIGGER LEVEL for a stable trace.
2. Adjust the X shift control to X1 and position the start of trace in the center of the Graticule. Adjust the value of the A.O.T. resistor R972 such that the sweep start voltage lies in the range +75 to +85V on each plate. It will be necessary to use the Test Oscilloscope for this task. Pull the X10 switch and repeat the procedure with R971 (AOT). It may be necessary to re-align the trace start for this purpose. The two X outputs to the tube should now limit at about +22V and +135V in each direction of sweep as the shift control is rotated on both X1 and X10.

5.5.14 ADJUSTMENT OF PRESET CONTRAST

Set the instrument as is Section 5.5.5 with the B timebase set to 10μs/cm and the HORIZONTAL MODE to A INTENS. BY B. The $\overline{B}$ TRIGGER LEVEL control should be at the B STARTS AFTER DELAY position. Adjust the preset contrast control R850 for a viewable contrast at normal intensity.

5.5.15 A TRIGGER BALANCE ADJUSTMENTS

1. Set the instrument to AC, CH1, A only, 0.1ms/cm and AUTO. Apply a 10kHz sinewave of about 6cms amplitude on the display, set the A TRIGGER LEVEL to centre and the input to AC TRIGGER coupling, with CH1 as source. Adjust R520 on the trigger p.c.b. for the trace to start approximately central in the waveform.
2. Set the TRIGGER COUPLING to DC, adjust R245 (DC TRIG BAL) on the Y preamplifier p.c.b. for no trigger level movement between DC coupling and AC coupling. Select the TRIGGER SOURCE to CH2, apply the input signal and repeat the procedure with R246. (CH2 DC TRIG BAL).
3. Select CH1 and CH2 ALTERNATE, Y inputs to AC and position both traces central on the graticule. Apply the same 10kHz input to both

channels. Select COMPOSITE TRIGGER SOURCE and adjust R311 (COMP. TRIG. BAL.) on the preamplifier p.c.b. for no trace movement between AC and DC trigger coupling.

4. Select CH1 and apply a low level signal to occupy about 2mm of trace. Adjust the trigger level for stable trigger and select the TRIGGER VIEW facility. Adjust the TRIGGER VIEW BALANCE R552 for a TRIGGER VIEW trace in the centre of the c.r.t.

5.5.16 B TRIGGER ADJUSTMENT

1. Select CH1, AC; TRIGGER SOURCES A & B to CH1, with TRIG COUPLING on AC. Set A timebase to 0.2ms/cm and B timebase to 0.1ms/cm. Select A INTENS BY B.
2. Adjust the A TRIGGER LEVEL control for a stable trigger with a 10kHz sinewave applied to CH1 (about 6cms).
3. Adjust the B TRIGGER LEVEL control for an intensified B trace. Change the HORIZONTAL MODE to B ONLY.
4. Set the B TRIGGER LEVEL control to centre and adjust R609 (B TRIG LEVEL BAL) for the start of trace to commence at the mid-point of the sinewave amplitude. Return to A ONLY and B STARTS AFTER DELAY.

5.5.17 EXT A COMPENSATION

1. Set TRIGGER SOURCE to EXT and the vertical mode to TRIGGER VIEW. Apply no HF of LF REJECT, and the TRIGGER COUPLING should be at DC. Insert a 1kHz square wave from the calibrator and adjust the trimmer C581 on the EXT attenuator p.c.b. for a square corner on the waveform.
2. Apply a 2V signal from the calibrator and insert a capacitance standardiser between the calibrator output and EXT A input. Adjust C583 for a Flat top on the square wave.

5.5.18 EXT B COMPENSATION

1. Set the 'B' TRIGGER LEVEL to center, 'B' COUPLING to DC and 'B' TRIGGER SOURCE to EXT.
2. Apply a 2.5V, 1kHz square wave to the EXT B input. Apply the Test Oscilloscope probe to one end of R614 (22Ω) and adjust C588 for a square corner.
3. Apply a 5V square wave via the capacitance standardiser and adjust C589 for a flat top. Return the B TRIGGER LEVEL to the B STARTS AFTER DELAY position.

5.5.19 A TIMEBASE CALIBRATION

1. Set the Y VERTICAL MODE to CH1 with input at DC, 1V/cm. Set the HORIZONTAL MODE to ' A INTENS BY B'. A TIME/cm to 1ms, B TIME/cm to 1μs.
2. Using the digital multimeter set on the 10V range apply to the tags of the DELAY control which connect to pins 9, 10 and 11 of SKV. Adjust R915 for a reading of 4.00 volts.
3. Set the DELAY control to minimum and adjust the X shift control for the intensified trace to begin at the first graticule vertical marking. Set the DELAY control to maximum and adjust R960 for the intensified trace to begin on the last graticule vertical marking. Return the DELAY control to minimum again and check the intensified trace alignment with the first vertical. Re-adjust R960 as necessary such that full adjustment of the DELAY control gives 10cms of movement on the intensified trace ±2mm.
4. Select 'A' only and apply 0.1ms markers from the TIMEMARK GENERATOR to the CH1 input. Adjust C722 to be central and R767 for 1 pulse/cm with the A TIME/cm set at 0.1ms/cm.
5. Apply 1μs markers, set the A TIME/cm to 1μs/cm and adjust C722 for 1 pulse/cm.
6. Apply 1ms markers, set the A TIME/cm to 1ms/cm and adjust R761 for 1 pulse/cm.
7. Apply 10μs/cm markers, set the TIME/cm to 0.1ms/cm, pull X10 switch and adjust R957 for one pulse/cm.
8. Set the trimmers C815 and C816 for minimum, and apply 10ns markers. The A TIME/cm should be set to 50ns/cm and the X10 switch pulled on, Set C815 and C816 by adjusting in equal amounts of capacitance on each such that the best trace linearity and accuracy are obtained. One pulse every 2cms should be displayed.

5.5.20 B TIMEBASE CALIBRATION

1. Select the HORIZONTAL MODE to 'B' and apply an input of 0.1ms markers. Set the A TIME/cm to 0.2ms/cm and the B TIME/cm to 0.1 ms/cm. The DELAY control should be set to zero and the 'B TRIGGER LEVEL' at the B STARTS AFTER DELAY position. Adjust R833 for one pulse/cm.
2. Apply 1μs markers, set the A TIME/cm to 2μs/cm and the B TIME/cm to 1μs/cm. Adjust C741 for 1 pulse/cm.
3. Apply 1ms markers, set the A TIME/cm to 2ms/cm and the B TIME/cm to 1ms/cm. Adjust R816 for 1 pulse/cm.
4. Set the A TIME/cm to 0.2ms/cm and the B TIME/cm to 0.1ms/cm. Select A & B ALTERNATE MODE, check that the A trace and B trace start within ± 2mm of each other. If not, change R827 (nominally 470Ω) AOT to suit. R827 should be changed to 560Ω if the B trace starts early or to 390Ω if it starts late.

5.5.21 X–Y CALIBRATION

1. Apply a 160mV 1kHz square wave signal at CH2 with the CH2 attenuator at 20mV/cm and input dc coupled. Select CH1 VERTICAL MODE

& GROUNDED, CH2 TRIGGER SOURCE AND DC TRIGGER COUPLING.

2. Select X–Y MODE and adjust R512 on the Trigger p.c.b. for exactly 8cms of horizontal display. (Note the calibration specification CH1 ± 15% CH2 ± 5%).

5.5.22 X–Y PHASE ALIGNMENT

1. Select CH2 display. Apply 5cms of 50kHz reference signal from an HF signal generator. A 45° line trace should now be visible on the c.r.t.
2. Increase the frequency to 500kHz and the line may be observed to open out to an elipse. Adjust the value of C506 (220pF) AOT for the elipse to close to a line again. Check that the line does not separate more than 2mm for frequencies up to 500kHz.

5.6 CALIBRATION PROCEDURE WITH DM3010 OPTION

NOTE:– It is assumed that the oscilloscope has been set according to the calibration details and that the internal set up procedure for the DM3010 has been followed in accordance with the DM3010 handbook.

5.6.1 TIMEBASE–TIME MEASUREMENT CALIBRATION

This setting procedure for the timebase with the DM3010 involves some repetition of oscilloscope adjustments described in Section 5.5 of this handbook but with the special requirements of the add on DVM and the greater setting accuracy needed. All variable controls should be set to the CAL positions.

1. Select CH1 VERTICAL MODE with INPUT COUPLING at DC and Y sensitivity at about 1V/cm (suitable to display about 5cm of Timemark Generator amplitude).
2. Insert the Timemark Generator to CH1 input. Set the HORIZONTAL MODE to A INTENS BY B. Set the A TIME/cm to 0.1ms and the B TIME/cm to 1μs. Apply 10μs markers.
3. Set the DELAY control to near to minimum on the oscilloscope and the v/t control on the DM3010 control to minimum. Select TIME MEASURE and INPUT SCOPE on the DM3010.
4. Pull the X X10 switch and observe the bright-ups at the beginning of the sweep. Adjust R96 on the DM3010 for alignment of the two bright-ups. The slope of the marker signal is useful for achieving this. Adjust the oscilloscope DELAY control to align with the leading edge of the first marker, and then R96 for coincidence.
5. Turn the front panel v/t control to its fully clockwise end. Using the 4½ digit DVM, measure the voltage between pin 11 (the wiper of R18) and pin 10 (0V). Adjust R54 in the DM3010 for a reading of 4.000V.
6. Apply 0.1ms markers. Return the X10 switch to the X1 position. Increase the v/t control to maximum. The DM3010 should display 1.000ms. Adjust R960 (X AMPLIFIER X1 GAIN) for the two bright-ups to appear exactly 10cms apart. Adjust preset R767 so that 1 marker/cm is displayed.
7. Apply 0.5ms markers. Advance the DELAY control (OS3500) such that the first bright-up occurs on the first available marker and check that the 20th marker is intensified by the second bright-up. Now press the B ONLY mode. Readjust R767 for exact coincidence of the two B traces.
8. Return the v/t control to read 0.500ms and check that the 10th marker is display. (Return to the A INTENS B position to check this). Adjust the v/t control for coincidence of the 1st and 10th markers on the B traces and check that the DM3010 reads 0.500ms ±7 digits. Return the v/t control to maximum.
9. Set the A TIME/cm switch to 1μs and the B TIME/cm to 100ns. Apply 500ms markers. Select the A INTENS BY B mode. Set the DELAY control for the first bright-up to occur on the first available marker. With the v/t control on the DM3010 set at maximum, adjust C722 on the OS3500 timebase p.c.b. for two markers/cm to be displayed. The second bright-up should now occur coincident with the 20th marker. Select the B ONLY mode and apply final adjustment to C722 so that the two B traces coincide. The DM3010 should now read 10.00μs.
10. Set the DM3010 v/t control so that the 10th marker is displayed. (Referring back to the A INTENS BY B position) and align the two B traces. The DM3010 should read 5.00μs ± 7 digits.
11. Since the presets C722 and R767 are slightly interactive (by approx ± 0.1%) it is best to recheck the calibration at step 7, readjusting R767 if necessary.
12. Set the A TIME/cm switch back to 1μs/cm again and apply 100ns markers. Select A INTENS BY B (or A ONLY) and pull the X10 switch on the X SHIFT control. Adjust R957 (XX10 GAIN CONTROL) for 1 marker/cm.
13. Set the A TIME/cm switch and the B TIME/cm switch to 50ns. Apply 10ns markers. With the X10 function still selected and the X SHIFT control approximately central adjust the trimmers C815, C816 for one marker every two centimetres. This is most easily done by firstly setting the trimmers to minimum capacitance and then adjusting each by the same amount of capacitance until the best linearity and accuracy can be obtained.
14. Select the A INTENS BY B position and return the X SHIFT switch to the X1 position. With the same setting as for the previous test, adjust the

v/t control on the DM3010 to MINIMUM. Set the DELAY control (OS3500) to align with the leading edge of the first available marker. Pull the X10 control again and select the B ONLY mode. By connecting a small trimmer 0–20pF across the appropriate select on Test pins C754 or C755. Set the two B traces for alignment. Remove the trimmer measure its value and replace it by a fixed capacitor of nearest preferred tolerance. The B trace alignment should now be within 1ns. This adjustment equalizes for differential delay which may exist between the two comparators IC710a and IC710b. Note that if B trace coincidence is already within 1ns no adjustment need be made.

15. Apply 0.5ms markers. Set the A TIME/cm to 2ms and the B TIME/cm to 0.1ms. Select A INTENS BY B and return the X10 switch to the X1 position. Set the DM3010 v/t control to maximum. Adjust the DELAY control (OS3500) to align the first bright-up on the first available marker. Adjust R761 for 2 markers/cm with the second bright-up occuring on the 20th marker. Now select B ONLY adjust R761 for coincidence of the B traces. The DM3010 should now indicate 10.00ms.
16. Set the DM3010 v/t control to display 10 marker pulses (using the A INTENS BY B mode). Align the v/t control for coincidence of the B traces on the B ONLY mode and check that the DM3010 reads 5.00ms ± 7 digits.
17. Check the DM3010 calibration with the OS3500 oscilloscope on the remaining timebase ranges to be within the specification accuracy. Also check that the full scale indication of the DM3010 is 10 times the A TIME/cm reading.

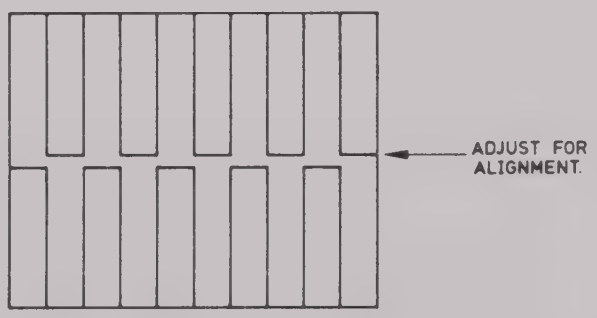
TIMEBASE – FREQUENCY CALIBRATION

The additional calibration is required for the $\frac{1}{T}$ (FREQUENCY) function. Correct operation of each range should be checked by setting the v/t control for a 1cm delay in the TIME mode and the check each A Timebase range for an equivalent full scale display in the $\frac{1}{T}$(FREQUENCY) mode. Repeat for 10cm display, checking for the equivalent $\frac{1}{10}$ full scale display.

5.6.2 Y DEFLECTION – VOLTAGE CALIBRATION

1. Select A ONLY, 0.5ms/cm and CH2 display and trigger, AC INPUT COUPLING. Select 'SCOPE' input and volts measurement. Set the CH2 attenuator switch to 20mV/cm.
2. Apply a 200mV calibration signal (1kHz square wave) and set the v/t control on the DM3010 to maximum. Adjust the Y CH2 shift approximately to set the top peaks of the lower (scope Y shift) trace with the bottom peaks of the DM3010 Y–shifted trace approximately in the center of the c.r.t. display. Adjust R284 so that the top 'SCOPE' Y shift peaks occur on the same horizontal line as the DM3010 bottom peaks (as set by the v/t control). See Fig.below. It is useful to adjust to the horizontal center line of the graticule to achieve this.
   The DM3010 should now read 100.0mV.
3. Now apply a 5mV calibration signal and re-adjust the DM3010 v/t control for trace coincidence as in step 2. Check that the DM3010 reads 50.0mV ± 7, 12 digits.
4. Check all the remaining CH2 VOLTS/cm ranges for calibration accuracy as per step 2 to be within specification noting that the F.S.D. of the DM3010 reads 10 scale divisions in each case.

NOTE that the dynamic range of the oscilloscope amplifier limits the accuracy at extremes of signal input, i.e. beyond 8cm deflection from the center. For this reason the above calibration uses a 10cm pk/pk signal AC coupled. DC coupling of a unipolar 10cm signal would cause inaccuracy.



ABBREVIATIONS USED FOR COMPONENT DESCRIPTIONS

RESISTORS

CC	Carbon Composition	½W	10%	unless otherwise stated
CF	Carbon Film	1/8W	5%	unless otherwise stated
MO	Metal Oxide	½W	2%	unless otherwise stated
MF	Metal Film	¼W	1%	unless otherwise stated
MG	Metal Glaze			
WW	Wire Wound	6W	5%	unless otherwise stated
CP	Control Potentiometer		20%	unless otherwise stated
PCP	Preset Potentiometer Type MPD,PC		20%	unless otherwise stated

CAPACITORS

CE(1)	Ceramic		+80% -25%	
CE(2)	Ceramic	500V	±10%	unless otherwise stated
SM	Silver Mica			
PF	Plastic Film		±10%	unless otherwise stated
PS	Polystyrene	63V	±2½%	unless otherwise stated
PE	Polyester		±10%	unless otherwise stated
PC	Polycarbonate			
E	Electrolytic (aluminium)		+50% -10%	
T	Tantalum		+50% -10%	

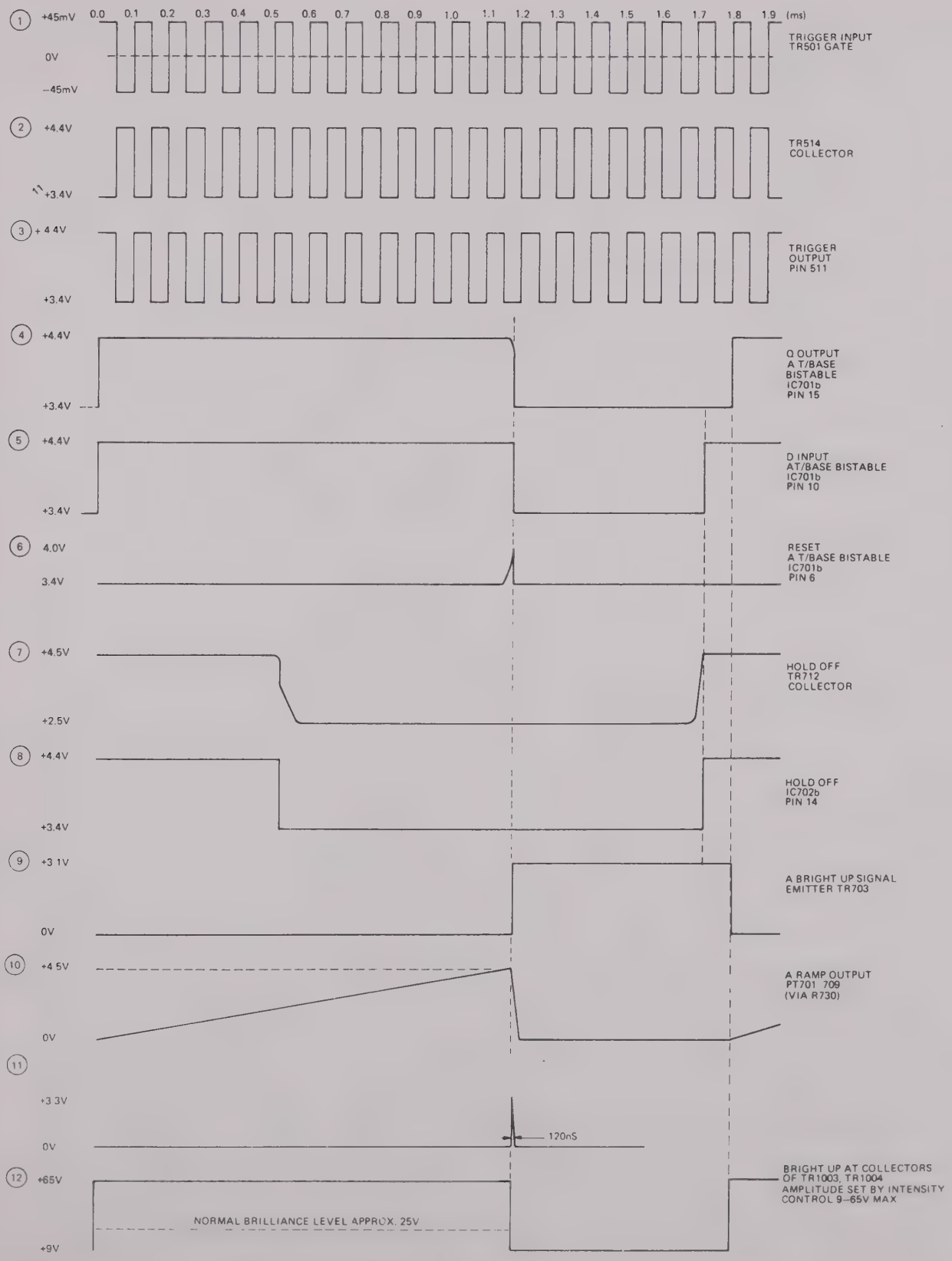


Fig. 2 T/B Waveforms Normal 'A' Sweep

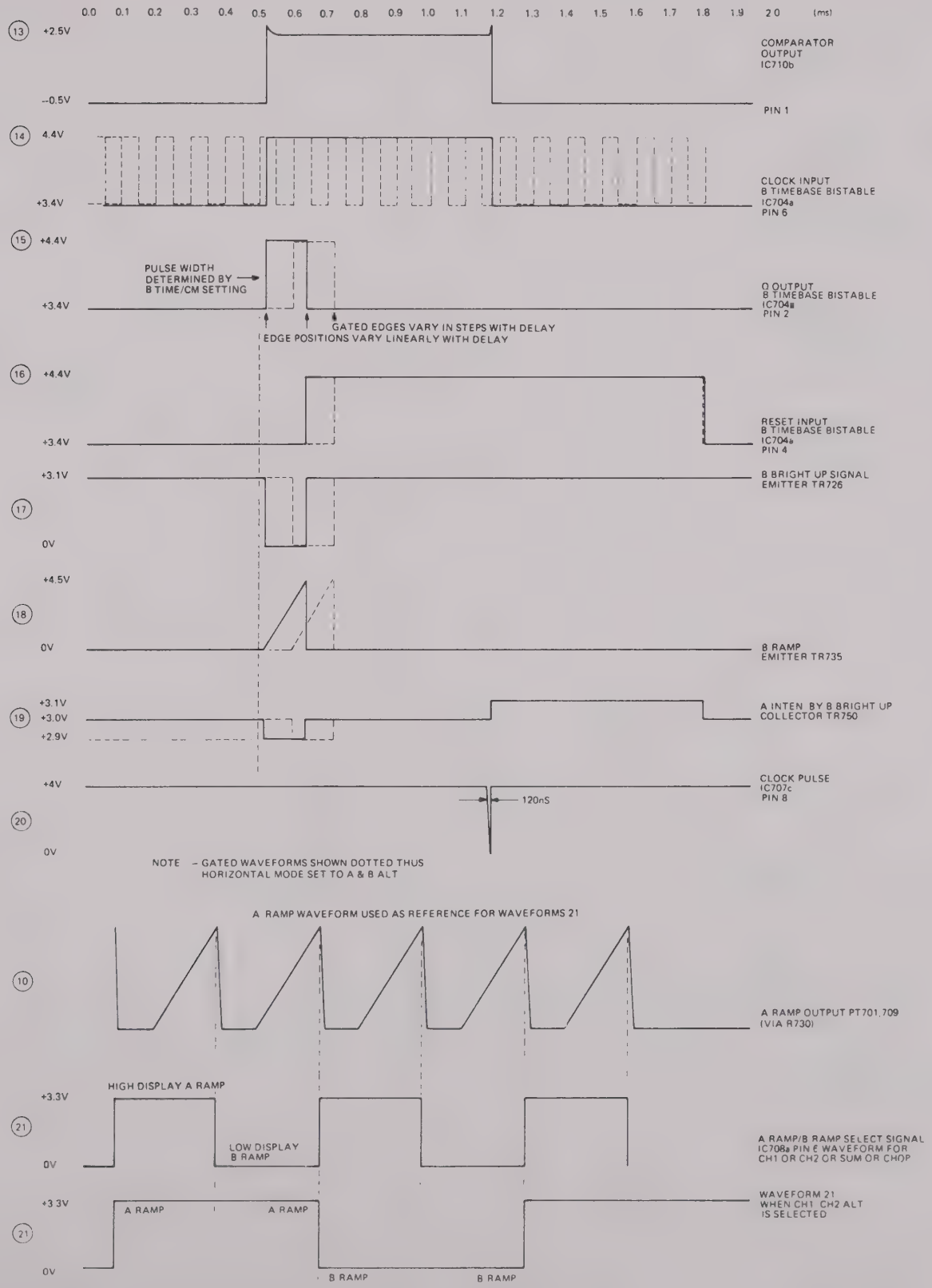
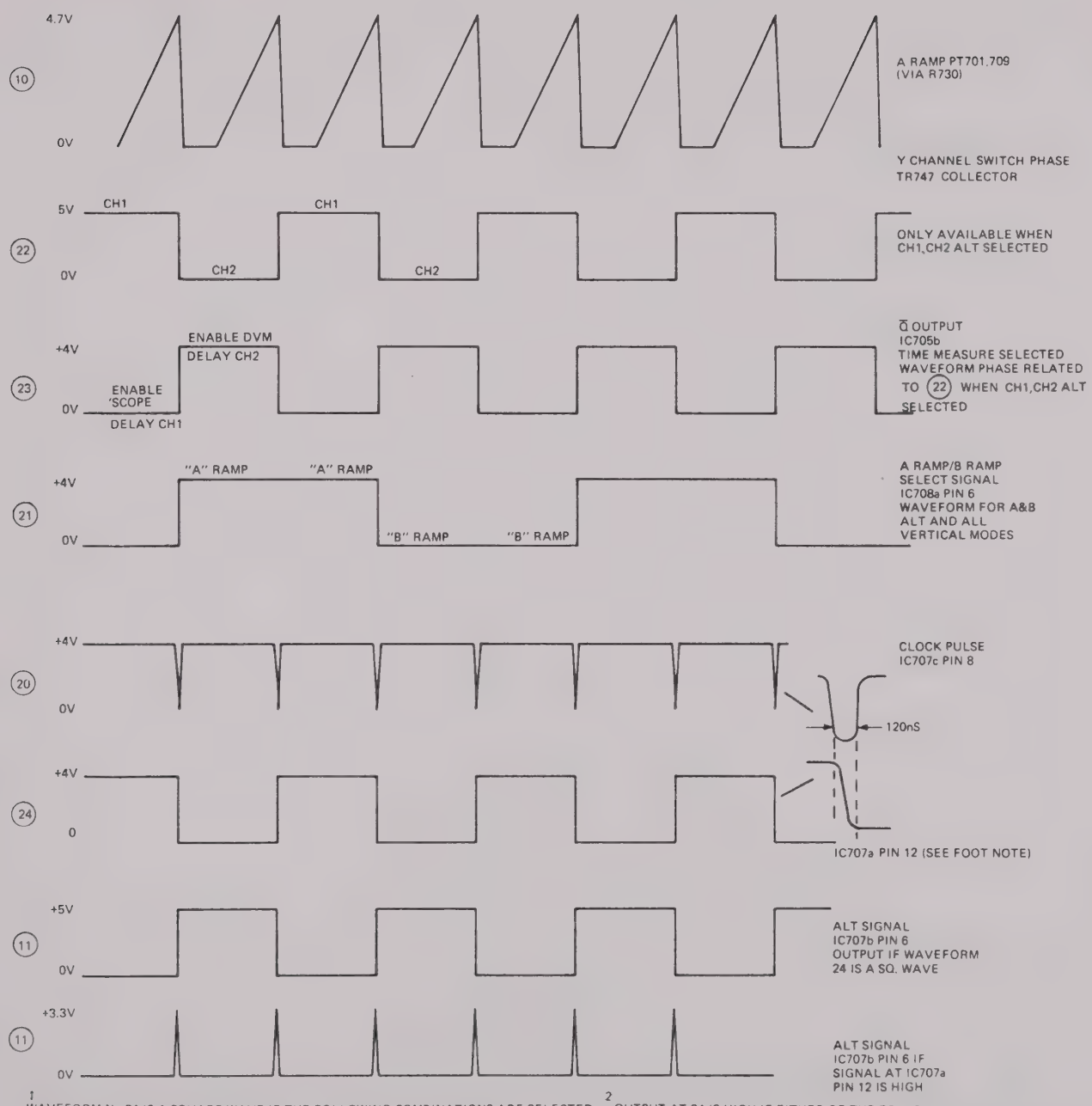


Fig. 3 T/B Waveforms Dual Operation



1 WAVEFORM No.24 IS A SQUARE WAVE IF THE FOLLOWING COMBINATIONS ARE SELECTED
CHOP & TRIG. VIEW AND EITHER A ONLY, B ONLY OR A INT B

2 OUTPUT AT 24 IS HIGH IF EITHER OF THE FOLLOWING ARE SELECTED:-

COMP TRIG
A & B ALT
VOLTS MEASUREMENT
NO MEASUREMENT
CH1, CH2, SUM OR ALT.

Fig. 4 T/B Waveforms DM3010 Time

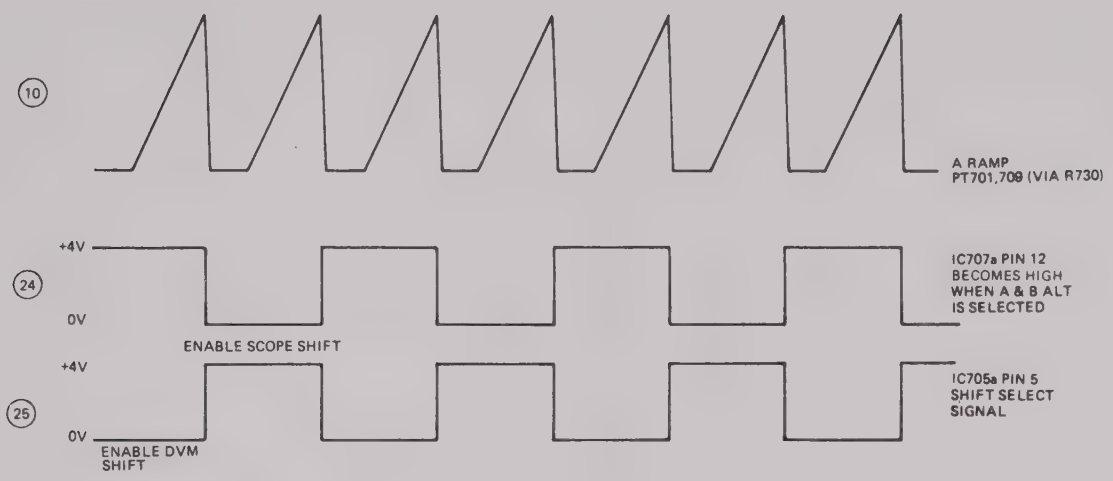


Fig. 5 T/B Waveforms DM3010 Voltage

OS3500 Y PRE AMP & Y LOGIC

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R101	10k1	MF	½W	37778
R102	10k1	MF	½W	37778
R103	111k	MF	½W	37779
R104	111k	MF	½W	37779
R111	2k2	CF		21802
R112	2k2	CF		21802
R113	2k2	CF		21802
R114	2k2	CF		21802
R115	47	CF		28714
R116	47	CF		28714
R117	50k	PCP		39268
R118	50k	PCP		39268
R119	10	CF		21793
R120	10	CF		21793
R121	10k	CF		21809
R122	10k	CF		21809
R123	10	CF		21793
R124	10	CF		21793
R125	1k	MF	2	38594
R126	1k	MF	2	38594
R127	100	CF		21794
R128	100	CF		21794
R129	820	CF		28724
R130	820	CF		28724
R131	47	CF		28714
R132	47	CF		28714
R133	100	CF		21794
R134	100	CF		21794
R135	1k	PCP		39233
R136	1k	PCP		39233
R137	10k	CF		21809
R138	10k	CF		21809
R139	10	CF		21793
R140	10	CF		21793
R141				
R142				
R143	39	CF		28713
R144	39	CF		28713
R145	10	CF		21793
R146	10	CF		21793
R147	2k	MF	2	38601
R148	2k	MF	2	38601
R149	2k	MF	2	38601
R150	2k	MF	2	38601
R151	5k	PCP		39234
R152	5k	PCP		39234
R153	2k2	CF		21802
R154	2k2	CF		21802
R155	18	CF		28709
R156	18	CF		28709
R157	680	CF		28723
R158	680	CF		28723
R159	680	CF		28723
R160	680	CF		28723
R161	18	CF		28709
R162	18	CF		28709
R163				
R164				
R165	360	MF	2	38583
R166	360	MF	2	38583
R167	360	MF	2	38583
R168	360	MF	2	38583
R169	2k7	CF		28726
R170	2k7	CF		28726
R171	390	CF		28722
R172	270	CF		28720
R173	390	CF		28722
R174	270	CF		28720
R175	2k	MF	2	38601
R176	2k	MF	2	38601
R177				
R178				
R179	47	CF		28714
R180	47	CF		28714
R181	1k2	CF		21800
R182	1k2	CF		21800
R183	270	MF	2	38580
R184	270	MF	2	38580
R185	270	MF	2	38580
R186	270	MF	2	38580
R187	180	MF	2	38576
R188	180	MF	2	38576
R189	15	CF		28708
R190	15	CF		28708
R191	56	CF		28715
R192	56	CF		28715
R193	56	CF		28715
R194	56	CF		28715
R195	33	CF		28712
R196	33	CF		28712
R197	1k5	CF		21801
R198	1k5	CF		21801
R199				
R200				
R201	1k5	CF		21801
R202	1k5	CF		21801
R203	51	MF	2	38563
R204	51	MF	2	38563
R205	56	CF		28715
R206	56	CF		28715
R207	430	MF	2	38585
R208	300	MF	2	38581
R209	56	CF		28715
R210	56	CF		28715
R211	47	CF		28714
R212	47	CF		28714
R213	47	CF		28714
R214	47	CF		28714
R215	100	CF		21794

OS3500 Y PRE AMP & LOGIC (Cont)

Ref	Value	Description	Tol %±	Part No
RESISTORS (Cont)				
R216	100	CF		21794
R217				
R218	1k5	CF		21801
R219	390	CF		28722
R220	390	CF		28722
R221	100	PCP		39230
R222	100	PCP		39230
R223	27	CF		28711
R224	27	CF		28711
R225	100	CF		21794
R226	100	CF		21794
R227	100	CF		21794
R228	100	CF		21794
R229	5k6	CF		21806
R230	5k6	CF		21806
R231	5k	PCP		39234
R232	5k	PCP		39234
R233	560	CF		21798
R234	560	CF		21798
R235	33	CF		28712
R236	33	CF		28712
R237	8k2	CF		21808
R238	8k2	CF		21808
R239	33	CF		28712
R240	33	CF		28712
R241	560	CF		21798
R242	560	CF		21798
R243	10	CF		21793
R244	10	CF		21793
R245	1k	PCP		39233
R246	1k	PCP		39233
R247	1k2	CF		21800
R248	1k2	CF		21800
R249	100	CF		21794
R250	100	CF		21794
R251	820	CF		28724
R252	820	CF		28724
R253	1k5	CF		21801
R254	1k5	CF		21801
R255	47	CF		28714
R256	47	CF		28714
R257	100	CF		21794
R258	100	CF		21794
R259	820	CF		28724
R260	820	CF		28724
R261	1k5	CF		21801
R262	1k5	CF		21801
R263	100	CF		21794
R264	100	CF		21794
R265	5k6	CF		21806
R266	5k6	CF		21806
R267	1k8	CF		28725
R268	68	CF		28716
R269	1k8	CF		28725
R270	68	CF		28716
RESISTORS (Cont)				
R271	1k	CF		21799
R272	5k6	CF		21806
R273	5k6	CF		21806
R279	1k3	MF	2	38597
R280	560	CF		21798
R281	560	CF		21798
R282	1k3	MF	2	38597
R283	220	CF		21796
R284	500	PCP		39232
R285	680	MF	2	38590
R286	680	MF	2	38590
R287	1k5	CF		21801
R288				
R289	1k8	MF	2	38600
R290	10k	CF		21809
R291	10k	CF		21809
R292	10	CF		21793
R293	1k2	CF		21800
R294	10	CF		21793
R295	1k	CF		21799
R296	10	CF		21793
R297	5k6	CF		21806
R298	6k8	CF		21807
R299	5k6	CF		21806
R300	390	CF		28722
R301	300	MF		38581
R302	150	CF		28719
R303	100	CF		21794
R304	47	CF		28714
R305	47	CF		28714
R306	300	MF	2	38581
R307	330	CF		28721
R308	47	CF		28714
R309	10	CF		21793
R310	1k5	CF		21801
R311	1k	PCP		39233
R312	100	CF		21794
R313	56	CF		28715
R314	680	CF		28723
R315	680	CF		28723
R316	56	CF		28715
R317	1k	CF		21799
R318	10	CF		21793
R319	47	CF		28714
R320	1k	CF		21799
R321	330	CF		28721
R322	330	CF		28721
R323	180	MF	2	38576
R324	1k	CF		21799
R325	1k	CF		21799
R326	100	CF		21794
R327	51	MF	2	38563
R328	100	CF		21794
R329	33	CF		28712

OS3500 Y PRE AMP & LOGIC (Cont)

Ref	Value	Description	Tol %±	Part No
RESISTORS (Cont)				
R330	33	CF		28712
R331	560	CF		21798
R332	820	CF		28724
R333	33	CF		28712
R334	33	CF		28712
R335	560	CF		21798
R336	4k7	CF		21805
R337	4k7	CF		21805
R338	100	CF		21794
R339	1k	CF		21799
R340	1k	CF		21799
R341	100	CF		21794
R342	10k	CF		21809
R343	1k	CF		21799
R344	4k7	CF		21805
R345	6k8	CF		21807
R346	2k2	CF		21802
R347	10k	CF		21809
R348	3k3	CF		21803
R349	2k7	CF		28726
R350	820	CF		28724
R351	470	CF		21797
R352	2k2	CF		21802
R353	100	CF		21794
R354	680	CF		28723
R355	5k6	CF		21806
R356	68	CF		28716
R357	10	CF		21793
R358				
R359				
RN301		Resistor Network		36459
CAPACITORS				
C100				
C101	2/15pF	Trimmer		40554
C102	2/15pF	Trimmer		40554
C103	2/5pF	Trimmer		40301
C104	2/5pF	Trimmer		40301
C105	2/15pF	Trimmer		40554
C106	2/15pF	Trimmer		40554
C107	2/10pF	Trimmer		40302
C108	2/10pF	Trimmer		40302
C109	2/5pF	Trimmer		40301
C110	2/5pF	Trimmer		40301
C111	10nF	CE(2)	250V	42569
C112	10nF	CE(2)	250V	42569
C113	10nF	CE(2)	250V	42569
C114	10nF	CE(2)	250V	42569
C115	5.6pF	CE(2)		22361
C116	5.6pF	CE(2)		22361
C117	22µF	E	25V	32181
C118	22µF	E	25V	32181
C119	10nF	CE(2)	250V	42569
C120	10nF	CE(2)	250V	42569

Ref	Value	Description	Tol %±	Part No
CAPACITORS (Cont)				
C121	10nF	CE(2)	250V	42569
C122	10nF	CE(2)	250V	42569
C123	10nF	CE(2)	250V	42569
C124	10nF	CE(2)	250V	42569
C125	10nF	CE(2)	250V	42569
C126	10nF	CE(2)	250V	42569
C127	3/45pF	Trimmer		36274
C128	3/45pF	Trimmer		36274
C129	10nF	CE(2)	250V	42569
C130	10nF	CE(2)	250V	42569
C131	470pF	CE(2)		22383
C132	470pF	CE(2)		22383
C133	470pF	CE(2)		22383
C134	470pF	CE(2)		22383
C135	2.2nF	CE(2)		22389
C136	2.2nF	CE(2)		22389
C137	1.5pF	CE(2)		40356
C138	1.5pF	CE(2)		40356
C139	2.2nF	CE(2)		22389
C140	2.2nF	CE(2)		22389
C141	10nF	CE(2)	250V	42569
C142	10nF	CE(2)	250V	42569
C143	10nF	CE(2)	250V	42569
C144	10nF	CE(2)	250V	42569
C145	3/45pF	Trimmer		36274
C146	3/45pF	Trimmer		36274
C147				
C148	27pF	CE(2)		22369
C149	56pF	CE(2)		22373
C150	56pF	CE(2)		22373
C151	10nF	CE(2)	250V	42569
C152	10nF	CE(2)	250V	42569
C153	10nF	CE(2)	250V	42569
C154	10nF	CE(2)	250V	42569
C155	10nF	CE(2)	250V	42569
C156	10nF	CE(2)	250V	42569
C157	10nF	CE(2)	250V	42569
C158	10nF	CE(2)	250V	42569
C159, C160	Not Used			
C161	10nF	CE(2)	250V	42569
C162	10nF	CE(2)	250V	42569
C163	10pF	CE(2)		22364
C164	10pF	CE(2)		22364
C165	10nF	CE(2)	250V	42569
C166	10nF	CE(2)	250V	42569
C167	33µF	E	16V	32173
C168	10nF	CE(2)	250V	42569
C169	10nF	CE(2)	250V	42569
C170	10nF	CE(2)	250V	42569
C171	33µF	E	16V	32173
C172	33µF	E	16V	32173
C300	Not Used			
C301	1.5pF	CE(2)		40356

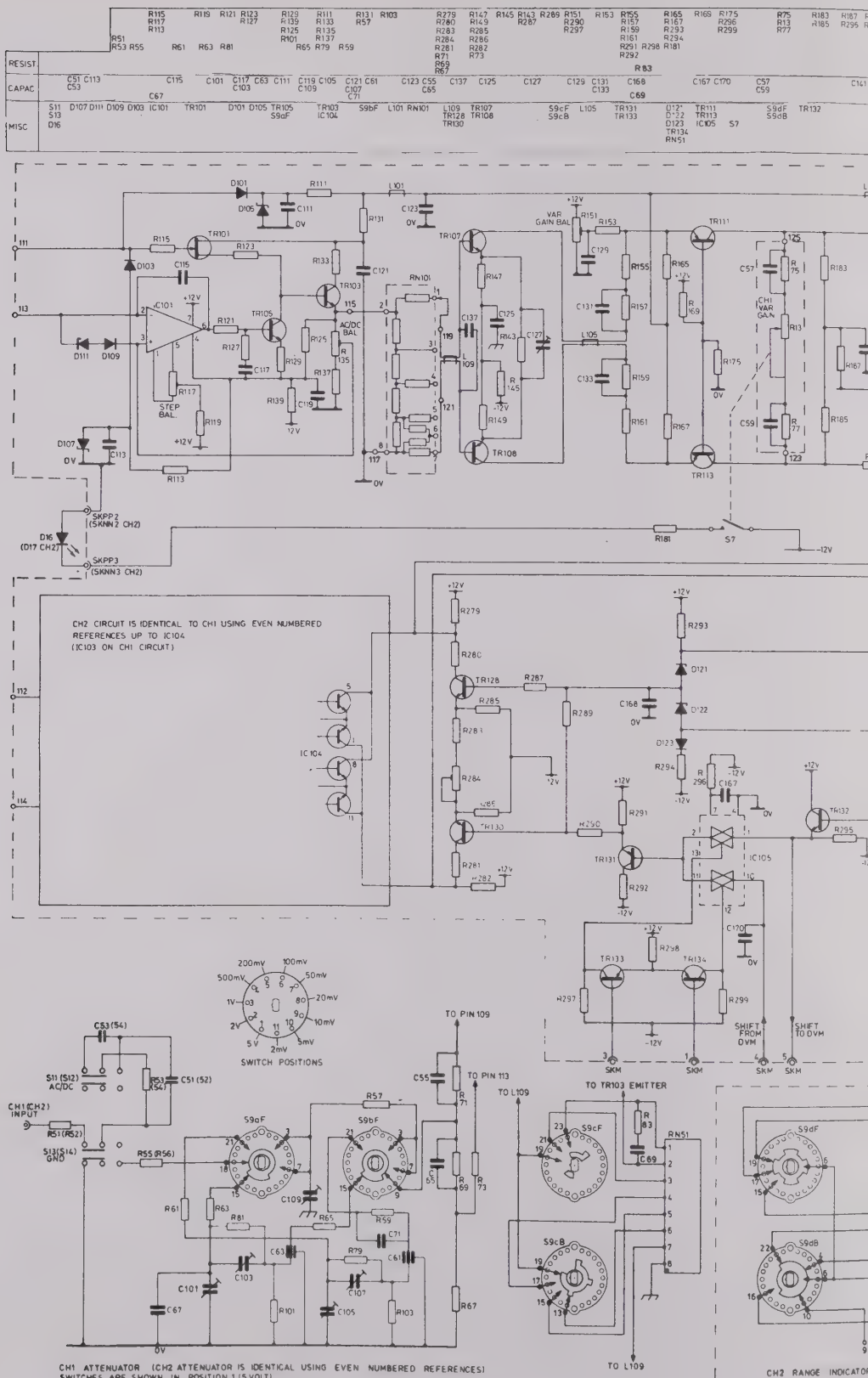
OS3500 Y PRE AMP & LOGIC (Cont)

Ref	Value	Description	Tol %±	Part No
CAPACITORS (Cont)				
C302				
C303	10nF	CE(2)	250V	42569
C304	1.5nF	CE(2)		22388
C305	1.5nF	CE(2)		22388
C306	10nF	CE(2)	250V	42569
C307				
C308	10nF	CE(2)	250V	22395
C309	100pF	CE(2)		22376
C310	10nF	CE(2)	250V	22395
C311	10nF	CE(2)	250V	22395
C312	10nF	CE(2)	250V	22395
C313	150pF	CE(2)		22378
C314	10nF	CE(2)	250V	22395
C315	560pF	CE(2)		22384
C316	10nF	CE(2)	250V	22395
C317	1μF	T	35V	34895
C318				
C319	5.6pF	CE(2)		22361
C320				
C321	10nF	CE(2)	250V	42569
C322	10nF	CE(2)	250V	22395
C323	10nF	CE(2)	250V	42569
C324				
C325	47μF	T	16V	39125
C326	10nF	CE(2)	250V	22395
C327	10nF	CE(2)	250V	22395
DIODES				
D101		FD300		35592
D102		FD300		35592
D103		FD300		35592
D104		FD300		35592
D105	3V3	ZENER	5	33923
D106	3V3	ZENER	5	33923
D107	3V3	ZENER	5	33923
D108	3V3	ZENER	5	33923
D109		IN3595		29330
D110		IN3595		29330
D111	2V7	ZENER		33921
D112	2V7	ZENER		33921
D121	4V7	ZENER		33927
D122	4V7	ZENER		33927
D123		IN4148		23802
D301		IN4148		23802
D302		IN4148		23802
D303		IN4148		23802
D304		IN4148		23802
D329		IN4148		23802
D330		IN4148		23802
D331		IN4148		23802
D332		IN4148		23802
D333		IN4148		23802

Ref	Value	Description	Tol %±	Part No
DIODES (Cont)				
D334		IN4148		23802
D335		IN4148		23802
D336		IN4148		23802
TRANSISTORS				
TR101		AE37		A4/40414
TR102		AE37		A4/40414
TR103		MPSH10		40315
TR104		MPSH10		40315
TR105		BF371		36275
TR106		BF371		36275
TR107		ZTX326A		41753
TR108		ZTX326A		41753
TR109		ZTX326A		41753
TR110		ZTX326A		41753
TR111		2N5771		38089
TR112		2N5771		38089
TR113		2N5771		38089
TR114		2N5771		38089
TR115		BF371		36275
TR116		BF371		36275
TR117		BF371		36275
TR118		BF371		36275
TR119		MPSH10		40315
TR120		MPSH10		40315
TR121		MPSH10		40315
TR122		MPSH10		40315
TR123		MPSH10		40315
TR124		MPSH10		40315
TR125		MPSH10		40315
TR126		MPSH10		40315
TR127		BC182B		33205
TR128		2N3904		24146
TR129		BC182B		33205
TR130		2N3904		24146
TR131		BC212		
TR132		BC182B		33205
TR133		BC212		29327
TR134		BC212		29327
TR301		2N5771		38089
TR302		2N5771		38089
TR303		2N5771		38089
TR304		2N5771		38089
TR305		BC182B		33205
TR306		BC182B		33205
TR307		2N5771		38089
INTEGRATED CIRCUITS				
IC101		LF355BN		42050
IC102		LF355BN		42050
IC103		SL3145		40784
IC104		SL3145		40784
IC105		MC14066B		40044

OS3500 Y PRE AMP & LOGIC (Cont)

Ref	Value	Description	Tol %±	Part No
INTEGRATED CIRCUITS (Cont)				
IC301		SL3145		40784
IC302		SL3145		40784
IC303		74LS00		43279
IC304		74LS10		36867
IC305		74LS112		36468
L101		Ferrite Bead FX1242		26986
L102		Ferrite Bead FX1242		26986
L103		Ferrite Bead FX1242		26986
L104		Ferrite Bead FX1242		26986
L105		Ferrite Bead FX1242		26986
L106		Ferrite Bead FX1242		26986
L107				
L108				
L109		Ferrite Bead FX1242		26986
L110		Ferrite Bead FX1242		26986
L111		Ferrite Bead FX1242		26986
L112		Ferrite Bead FX1242		26986
L113		Ferrite Bead FX1242		26986
L114		Ferrite Bead FX1242		26986
L115		Ferrite Bead FX1242		26986
L116		Ferrite Bead FX1242		26986
MISCELLANEOUS				
S101		Switch push button (INVERT)		A3/40742
S102		Switch push button (INVERT)		A3/40742
SKM		Connector 18 way		40017
SKN		Connector 18 way 3 way locking		41395


CH2 CIRCUIT IS IDENTICAL TO CH1 USING EVEN NUMBERED REFERENCES UP TO IC104 (IC103 ON CH1 CIRCUIT)
SWITCH POSITIONS
CH1 ATTENUATOR (CH2 ATTENUATOR IS IDENTICAL USING EVEN NUMBERED REFERENCES) SWITCHES ARE SHOWN IN POSITION 1 (5 VOLT)
CH2 RANGE INDICATOR
TO PIN 109
TO PIN 113
TO L109
TO TR103 EMITTER
SHIFT FROM DVM
SHIFT TO DVM
VAR GAIN BAL
CH1 VAR GAIN
STEP BAL
AC/DC BAL

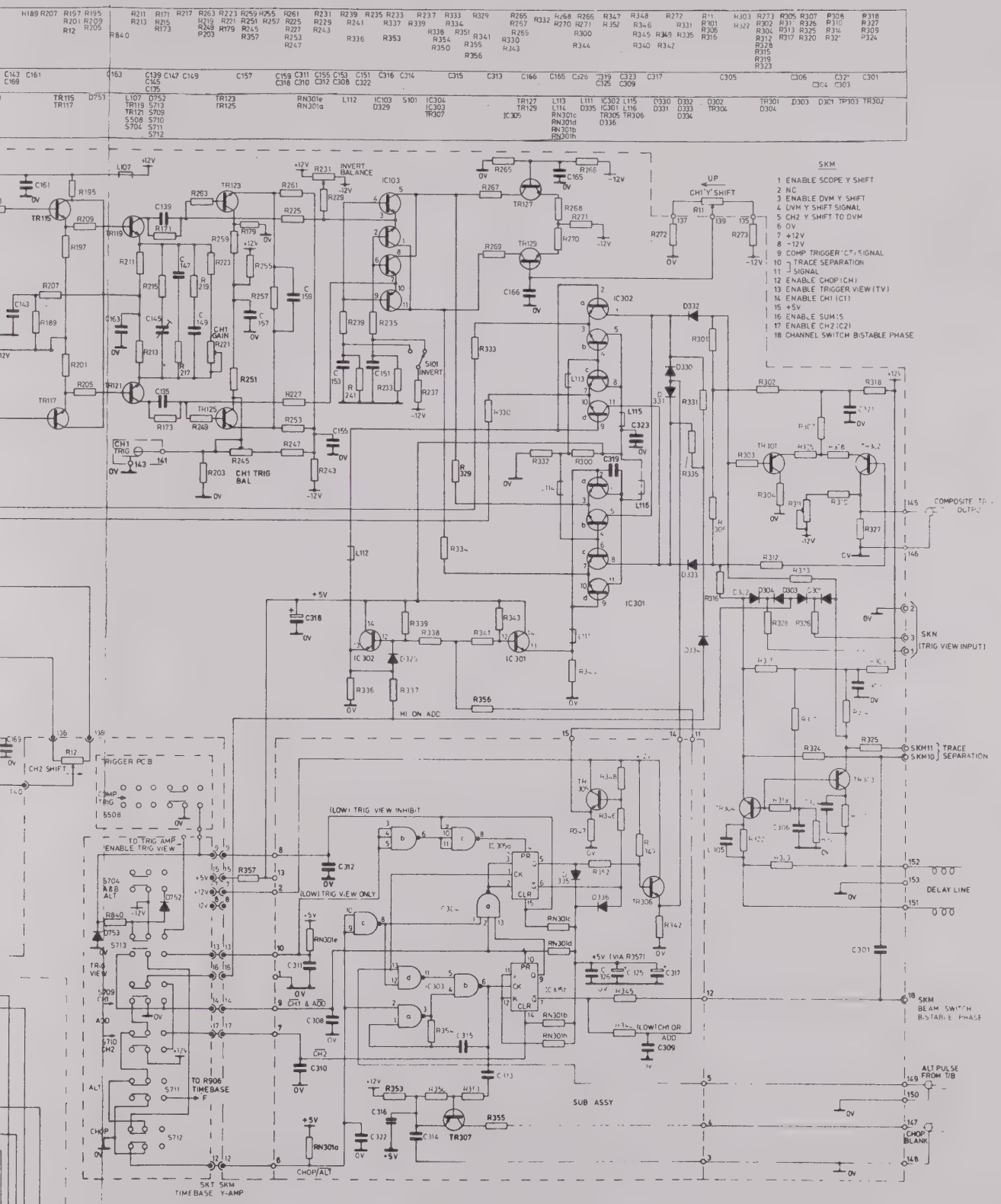


Fig. 6 Circuit Diagrams Y Pre-Amplifier

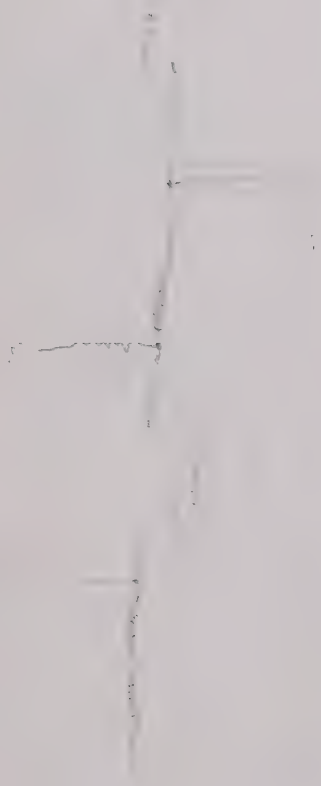
OS3500 'Y' OUTPUT (UP TO SER. No. 500)

Ref	Value	Description	Tol %±	Part No
RESISTORS				
R400	82	MF	2	38568
R401	82	MF	2	38568
R402	33	CF		28712
R403	33	CF		28712
R404	68	CF		28716
R405	68	CF		28716
R406	390	MF	2	38584
R407	390	MF	2	38584
R408			A.O.T.	
R409	560	CF		21798
R410	22	CF		28710
R411	56	CF		28715
R412	56	CF		28715
R413	10	CF		21793
R414	200	PCP		39231
R415	2k7	CP		21809
R416	22k	CF		21812
R417	680	CF		28723
R418	680	CF		28723
R419	220	MF	2	21796
R420	22	CF		28710
R421	820	CF		28724
R422	820	CF		28724
R423	18	CF		28709
R424	4k7	CF		21805
R425	270	CF		28720
R426	3k9	CF		21804
R427	3k9	CF		21804
R428	560	MF	2	38588
R429	560	MF	2	38588
R430				
R431	68	CF		28716
R432	68	CF		28716
R433	300	MF	2	38581
R434	120	CF		28718
R435	120	CF		28718
R436	470	CF		21797
R437	470	CF		21797
R438	1k2	CF		21800
R439	1k2	CF		21800
R440				
R441	47	CF		28714
R442	47	CF		28714
R443	120	MO		40317
R444	47	CF	5	18534
R445	47	CF	5	18534
R446	100	PCP		39230
R447	1k	CF		21799
R448	33	CF		28712
R449				
R450				
R451	47	CF		18534
R452	47	CF	½W	18534
R453	47	CF		28714
R454	10	CF		21793
R455	10	CF		21793
R456				
R457				
R458	510	MO	5 6W	40318
R459	510	MO	5 6W	40318
R460	33	CF		28712
R461	180	WW	5 2W	2210
R462	1k	CF		21799
R463	47	CF		28714
R464	10k	CP	Intensity	A4/38681
R465				
R466	1k	CP	Scale	A4/38680
R467	2k2	CP	Trace Rotate	A4/38678
R468	240	MO	2	39135
R469	3M6	MG	5 ½W	40327
R470	470	CF		21797
R471	470	CF		21797
R472	100k	PCP		39269
R473	1M	PCP		39431
R474	10	CF		21793
R475	1M	CP	Focus	A4/38679
R476				
R477	220k	CF		21823
R478	150	CF		28719
R479	470	CF		21797
R480	470	CF		21797
CAPACITORS				
C400	10nF	CE(2)	250V	22395
C401	10nF	CE(2)	250V	22395
C402				
C403	12pF	CE(2)		22365
C404	27pF	TRIMMER		36273
C405	47pF	CE(2)		22372
C406	2n2F	CE(2)		22389
C407	1nF	CE(2)		
C408	1nF	CE(2)		
C409	10nF	CE(2)	250V	22395
C410	2.2pF	SM	350V	815
C411	10nF	CE(2)	250V	22395
C412	1pF8	CE(2)	50V	36597
C413	1pF8	CE(2)	50V	36597
C414	10nF	CE(2)	250V	22395
C415	10nF	CE(2)	250V	22395
C416	10nF	CE(2)	250V	22395
C417	10nF	CE(2)	250V	22395
C418	10nF	CE(2)	250V	22395
C419	10nF	CE(2)	250V	22395
C420				
C421	10nF	CE(2)	250V	22395
C422	2½/45pF	TRIMMER		36274
C423	27pF	TRIMMER		36273
C424	2.2pF	CE(2)	50V	36598
C425				

OS3500 'Y' OUTPUT (UP TO SER. No. 500) (Cont)

Ref	Value	Description	Tol % ±	Part No
CAPACITORS (Cont)				
C426	10nF	CE(2)	250V	22395
C427	10nF	CE(2)	250V	22395
C428	10nF	CE(2)	250V	22395
C429	10nF	CE(2)	250V	22395
C430				
C434	10nF	CE(2)	250V	22395
C435	2.2pF	CE(2)	50V	36598
TRANSISTORS				
TR400		2N5771		38089
TR401		2N5771		38089
TR402		MPS H10		40315
TR403		MPS H10		40315
TR404				
TR405				
TR406		BFT95		41507
TR407		BFT95		41507
TR408		2N3866		27740
TR409		2N3866		27740
TR410				
TR411		2N3866		27740
TR412		2N3866		27740
TR413		BFY51		29329
TR414		BFX 88		23337

Ref	Value	Description	Tol % ±	Part No
DIODES				
D400		FH1100 or ZC2800		40352
D401		FH1100 or ZC2800		40352
D402		FH1100 or ZC2800		40352
D403		FH1100 or ZC2800		40352
D404	5V6	ZENER	5	33929
D405	3V6	ZENER	5	33929
D406		IN4148		23802
D407	91V	ZENER	5	40319
D408	9V1	ZENER	5	33934
D409	5V1	ZENER		33928
SOCKETS				
SKG		2 Way Lockable Socket		41391
SKH		4 Way Lockable Socket		41393
SKJ		2 Way Lockable Socket		41391
SKK		2 Way Socket Molex		37880
SKL		11 Way Socket Molex		40323
MISCELLANEOUS				
S400		Trace Locate		A3/40741
L400		Ferrite FX1242		26986
L401		Ferrite FX1242		26986
L402		Y Output Coil		A2/40771
L403		Y Output Coil		A2/40771



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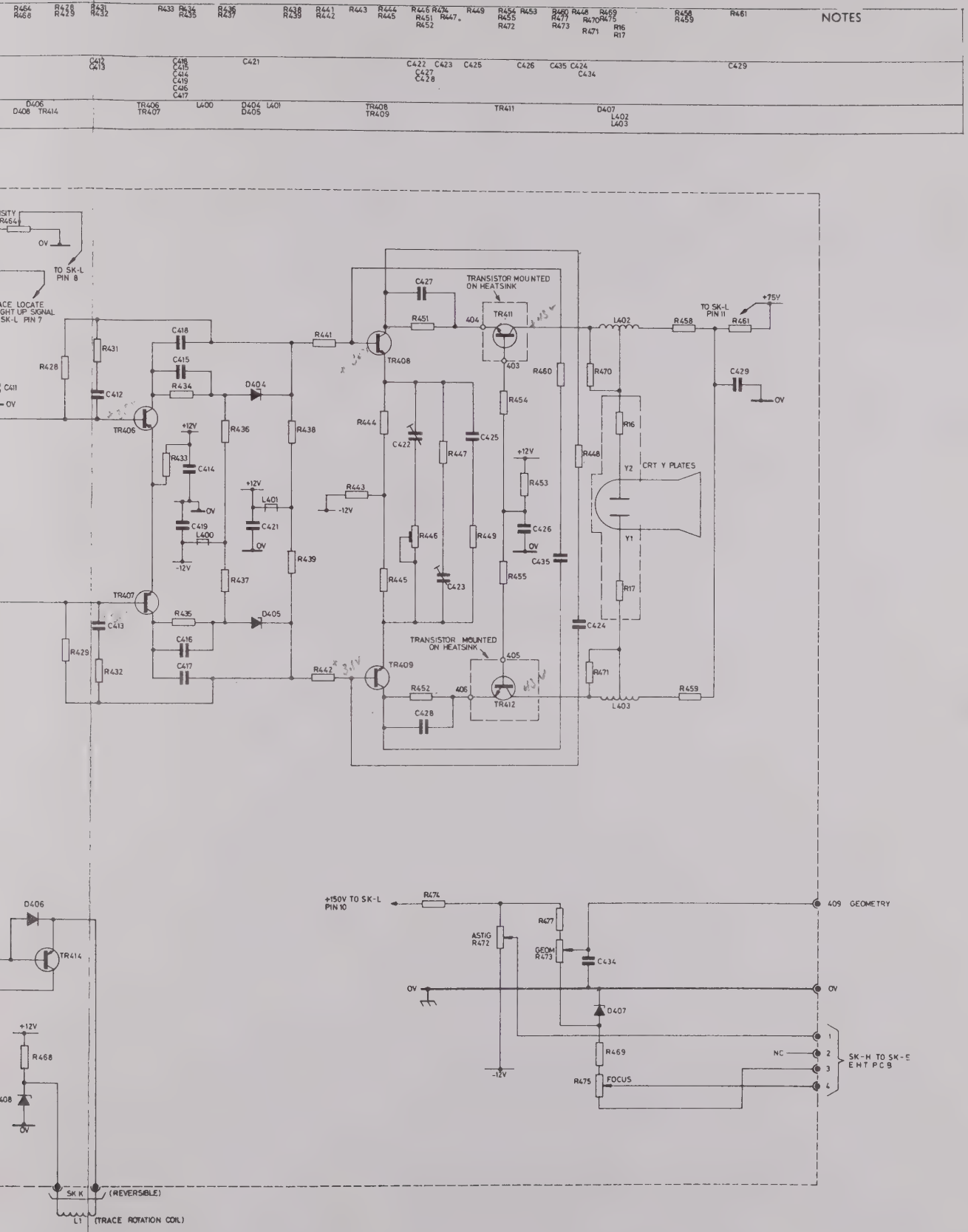


Fig. 7 Circuit Diagrams Y Output Amplifier

OS3500 TRIGGER P.C.B.

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R501	200k	MF	2	38649
R502	100	CF		21794
R503	560	CF		21798
R504	390	MF	2	38584
R505	390	MF	2	38584
R506	560	CF		21798
R507	560	CF		21807
R508	820	CF		28724
R509	1k5	MF	2	38598
R510	2k0	MF	2	38601
R511	910	MF	2	38593
R512	500	PCP		39232
R513	6k8	MF	2	38614
R514	12k	MF	2	38620
R515	120	CF		28718
R516	82	CF		28717
R517	1k8	CF		28725
R518	100k	CF		21819
R519	10	CF		21793
R520	20k	PCP		39235
R521	5k6	CF		21806
R522	22k	CP	'A' Trig Level	A4/38676
R523	4k7	CF		21805
R524	100	CF		21794
R525	5k6	CF		21806
R526	1k	MF	2	38594
R527	56	CF		28715
R528	47	CF		28714
R529	22	CF		28710
R530	22	CF		28710
R531	180	MF	2	38576
R532	180	MF	2	38576
R533	820	CF		28724
R534	560	CF		21798
R535	10k	CF		21809
R536	10	CF		21793
R537				
R538	22	CF		28710
R539	22	CF		28710
R540	39	CF		28713
R541	39	CF		28713
R542	680	CF		28723
R543	180	CF		21795
R544	180	CF		21795
R545	82	CF		28717
R546	82	CF		28717
R547	2k2	CF		21802
R548	560	CF		21798
R549	47k	CF		21815
R550	1k	MF	2	38594
R551	1k	MF	2	38594
R552	500	PCP		39232
R553	10	CF		21793
R555	10	CF		21793

Ref	Value	Description	Tol % ±	Part No
RESISTORS (Cont)				
R556	22	CF		28710
R558	22	CF		28710
R559	22	CF		28710
R560	10	CF		21793
R561	1k	CF		21799
R562	27	CF		28711
R563	27	CF		28711
R564	270	CF		28720
R565	270	CF		28720
R566	2k2	CF		21802
R567	470	CF		21797
R568	47	CF		28714
R569	330	CF		28721
R570	470	CF		21797
R571	470	CF		21797
R572	300	MF	2	38581
R573	560	CF		21798
R574	1k5	MF	2	38598
R575	1k2	MF	2	38596
R576	390	MF	2	38584
R577	390	CF		28722
R578				
R579				
R580	430	MF	2	38585
R581	10	CF		21793
R582	47k	CF		21815
R583	12k	CF		21810
R584	68k	CF		21816
R585	560k	CF		32359
R586	270	CF		28720
R587	100k	CF		21797
R588	100k	CF		21819
R589	10k	CF		21809
R590	56	CF		28715
R591	1k5	CF		21801
R592	8k2	CF		21808
R593	270	CF		28720
R594	3k9	CF		21804
R595	2k2	CF		21802
R596	680	CF		28723
R597	10	CF		21793
R598	1k	CF		21799
R599	47	CF		28714
R600				
R601	200k	MF	2	38649
R602	100	CF		21794
R603	390	MF	2	38584
R604	220	CF		21796
R605	560	CF		21798
R606	390	MF	2	38584
R607	3k3	CF		21803
R608	5k6	CF		21806
R609	20k	P.C.		39235
R610	5k6	CF		21806

OS3500 TRIGGER P.C.B. (Cont)

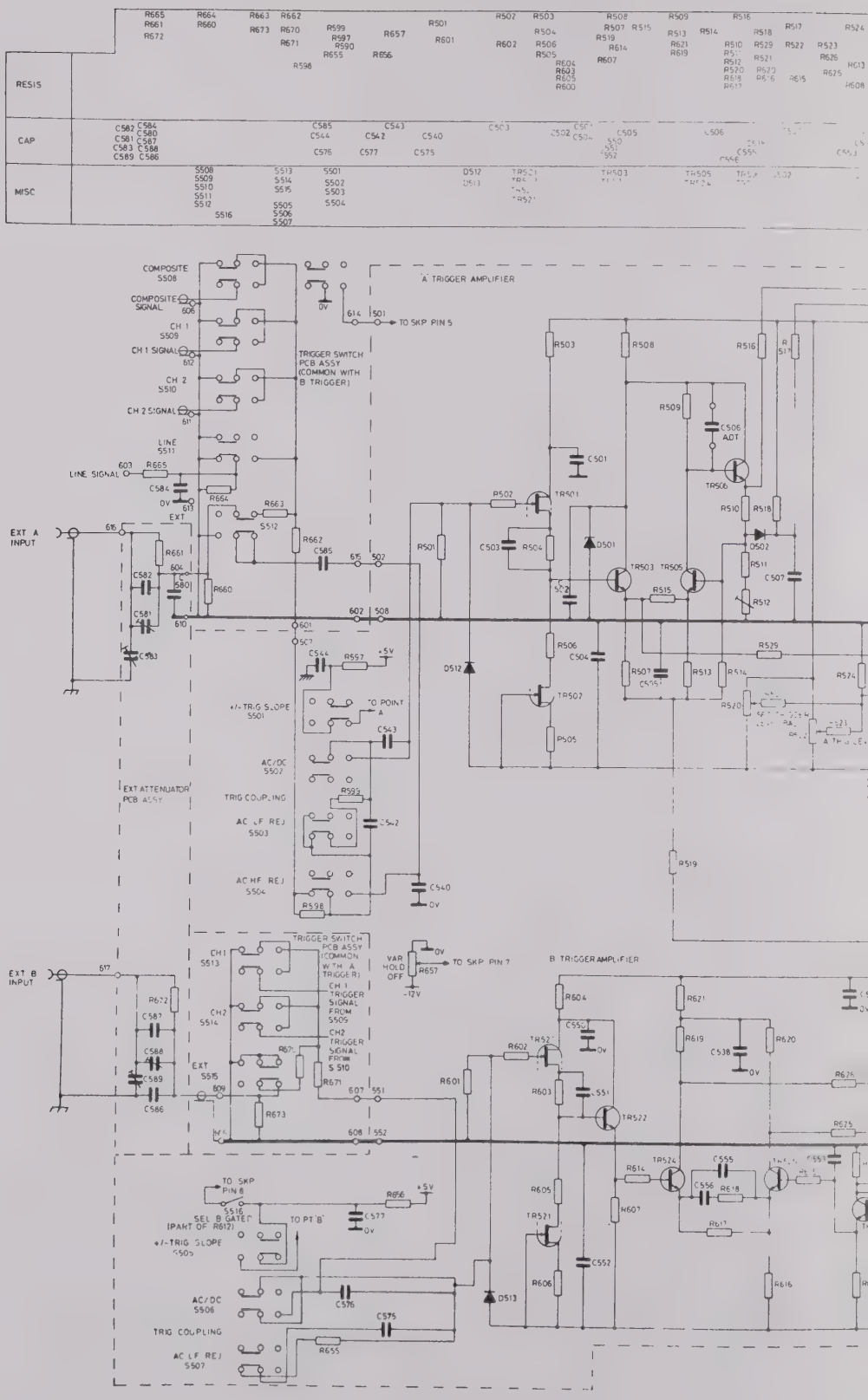
Ref	Value	Description	Tol %±	Part No
RESISTORS (Cont)				
R611	4k7	CF		21805
R612	22k	PCP	'B' Trig Level	A4/38677
R613	100	CF		21794
R614	22	CF		28710
R615	22	CF		28710
R616	1k	CF		21799
R617	47	CF		28714
R618	56	CF		28715
R619	180	MF	2	38576
R620	180	MF	2	38576
R621	820	CF		28724
R622				
R623				
R624				
R625	22	CF		28710
R626	22	CF		28710
R627	270	CF		28720
R628	270	CF		28720
R629	39	CF		28713
R630	39	CF		28713
R631	680	CF		28723
R632	22	CF		28710
R633	22	CF		28710
R634	270	CF		28720
R635	27	CF		28711
R636	27	CF		28711
R637	270	CF		28720
R638	1k	CF		21799
R639	10	CF		21793
R640	22	CF		28710
R641	2k2	CF		21802
R642	470	CF		21797
R643	47	CF		28714
R644	330	CF		28721
R645	470	CF		21797
R646	470	CF		21797
R647	300	MF	2	38581
R648	560	CF		21798
R649	390	MF	2	38584
R650	1k5	MF	2	38598
R651	1k2	MF	2	38596
R652	10	CF		21793
R653	10	CF		21793
R654	390	CF		28722
R655	47	CF		28714
R656	10	CF		21793
R657	47k	CP	Var. Hold Off	A4/38674
R658				
R660	200k		2 ¼W	38649
R661	900k		0.5	40743
R662	39		5 1/8W	28713
R663	82		5 1/8W	28717
R664	3k3		5 1/8W	21803
R665	3k3		5 1/8W	21803

Ref	Value	Description	Tol %±	Part No
DIODES (Cont)				
R670	82		5 1/8W	28717
R671	39		5 1/8W	28713
R672	900k		0.5	40743
R673	200k		2 ¼W	38649
CAPACITORS				
C501	10nF	CE(2)		22395
C502	10nF	CE(2)		22395
C503	10nF	CE(2)		22395
C504	10nF	CE(2)		22395
C505	10nF	CE(2)		22395
C506	220pr	PS	A.O.T.	22379
C507	10nF	CE(2)		22395
C508	27pF	CE(2)		22369
C509	22pF	CE(2)		22368
C510	220pF	CE(2)		22379
C511	10nF	CE(2)		22395
C512	1nF	CE(2)		22387
C513	10nF	CE(2)		22395
C514	4n7F	CE(2)		22393
C515	10nF	CE(2)		22395
C516	47pF	CE(2)		22372
C517	10nF	CE(2)		22395
C518	27pF	CE(2)		22371
C519	10nF	CE(2)		22369
C520	10nF	CE(2)		22395
C521				
C522	15pF	CE(2)		22366
C523	10nF	CE(2)		22395
C524	10nF	CE(2)		22395
C525	10nF	CE(2)		22395
C526	10nF	CE(2)		22395
C527				
C528	10µF	E	25V	32180
C529	10µF	E	25V	32180
C530	10µF	CE(2)		22395
C531	0.1µF	PE	100V	37018
C532	0.1µF	PE	100V	37018
C533	120pF	CE(2)		22377
C534	10nF	CE(2)		22395
C535	270pF	CE(2)		22380
C536	10nF	CE(2)		22395
C537	10nF	CE(2)		22395
C538	10nF	CE(2)		22395
C539				
C540	100pF	CE(2)		22376
C541				
C542	100pF	CE(2)		22376
C543	0.1µF	PE	100V	37018
C544	10nF	CE(2)		22395
C550	10nF	CE(2)		22395
C551	10nF	CE(2)		22395
C552	10nF	CE(2)		22395
C553	220pF	CE(2)		22379

OS3500 TRIGGER P.C.B. (Cont)

Ref	Value	Description	Tol % ±	Part No
CAPACITORS (Cont)				
C554	10nF	CE(2)		22395
C555	27pF	CE(2)		22369
C556	22pF	CE(2)		22368
C557	10nF	CE(2)		22395
C558	27pF	CE(2)		22369
C559	10nF	CE(2)		22395
C560	47pF	CE(2)		22372
C561	10nF	CE(2)		22395
C565	10nF	CE(2)		22395
C566				
C567	15pF	CE(2)		22366
C568	10nF	CE(2)		22395
C569	10nF	CE(2)		22395
C570	10nF	CE(2)		22395
C571	10nF	CE(2)		22395
C572	10μF	E	10V	40353
C573				
C574				
C575	100pF	CE(2)		22376
C576	0.1μF	PS	10 100V	37018
C577	10nF	CE(2)		22395
C581	6pF	TRIMMER		29421
C582	5.6pF	CE(2)		22361
C583	15pF	TRIMMER		32059
C584	10nF		250V	22395
C585	10nF		250V	22395
C586	56pF		500V	22373
C587	5.6pF	CE(2)		22361
C588	6pF	TRIMMER		29421
C589	15pF	TRIMMER		32059
DIODES				
D501	5V1	ZENER BZX79C	5	33928
D502		IN4148		
D503	3V3	ZENER BZX79C	5	33923
D504	9V1	ZENER BZX79C	5	33934
D505	6V2	ZENER BZX79C	5	33930
D506		IN4148		23802
D507		IN4148		23802
D508		IN4149		1949
D509		IN4149		1949
D510		IN4148		23802
D511		IN4148		23802
D512				

Ref	Value	Description	Tol % ±	Part No
DIODES (Cont)				
D513				
D514				
D515	9V1	ZENER BZX79C	5	33934
TRANSISTORS				
TR501 } TR502 }		Dual FET WD 392		A36243
TR503 } TR504 }		AE13 Transistor Matched Pair		A31254
TR505		2N3904		24146
TR506		2N3904		24146
TR507		2N5770		40347
TR508		2N5770		40347
TR509		2N5771		38089
TR510		2N5771		38089
TR511		BF371		36275
TR512		BF371		36275
TR513		MPS H10		40315
TR514		MPS H10		40315
TR515		2N2369		23307
TR516		2N3640		31781
TR517		2N2369		23307
TR518		BC182B		33205
TR519				
TR520 } TR521 }		Dual FET WD 392		A36243
TR522 } TR523 }		AE13 Transistor Matched Pair		A31254
TR524		2N5770		40347
TR525		2N5770		40347
TR526		2N5771		38089
TR527		2N5771		38089
TR528		MPS H10		40315
TR529		MPS H10		40315
INTEGRATED CIRCUITS				
IC501		MC10116		39244
IC502		MC10116		39244
MISCELLANEOUS				
S501–S504		A COUPLING		A3/40738
S505–S507		B COUPLING		A3/40737
S508–512				A3/40739
S513–515				A3/40740
SKP		13 Way Socket		39387
SKR		3 Way Locking Socket		39222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CAP
MISC
COMPOSITE S508
COMPOSITE SIGNAL
CH 1 S509
CH 1 SIGNAL
CH 2 S510
CH 2 SIGNAL
LINE S511
LINE SIGNAL
EXT S512
EXT A INPUT
EXT B INPUT
TRIGGER SWITCH PCB ASSY (COMMON WITH B TRIGGER)
A TRIGGER AMPLIFIER
B TRIGGER AMPLIFIER
TO SKP PIN 5
TO SKP PIN 7
TO SKP PIN 8
TO PT 'A'
TO PT 'B'
+/- TRIG SLOPE S501
AC/DC S502
TRIG COUPLING
AC LF REJ S503
AC HF REJ S504
SEL B GATE S516
(PART OF R612)
EXT ATTENUATOR PCB ASSY
CH1 S513
CH2 S514
EXT S515
CH 1 TRIGGER SIGNAL FROM S505
CH2 TRIGGER SIGNAL FROM S510
VAR HOLD OFF R657
+5V
-12V
0V

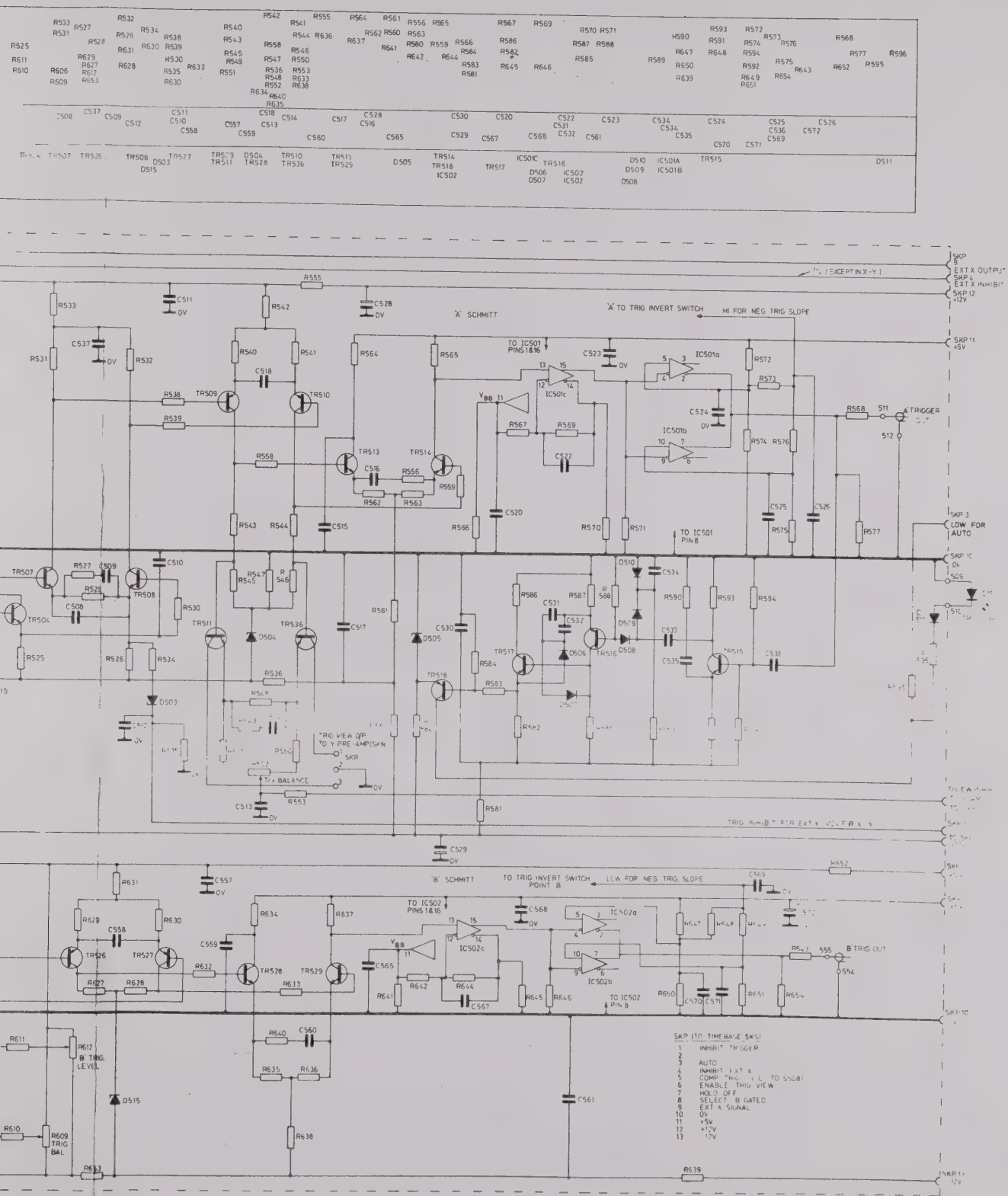


Fig. 8 Circuit Diagrams Trigger

OS3500 TIMEBASE

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R700				
R701	10k	CF		21809
R702	2k2	CF		21802
R703	180	CF		21795
R704				
R705				
R706				
R707	2k2	CF		21802
R708	4k7	CF		21805
R709	270	CF		28720
R710	1k2	MF		38596
R711	470	CF		21797
R712	3k3	MF	2	38606
R713	3k9	CF		21804
R714	180	CF		21795
R715	2k2	CF		21802
R716	1k5	CF		21801
R717				
R718				
R719	3k3	CF		21803
R720	390	CF		28722
R721	1k	CF		21799
R722	680	CF		28723
R723	680	CF		28723
R724	1k	CF		21799
R725	1k2	CF		21800
R726	360	MF	2	38583
R727	1k5	CF		21801
R728	3k3	CF		21803
R729	220	CF		21796
R730	10	CF		21793
R731	100	CF		21794
R732	10	CF		21793
R733	820	MF	2	38592
R734	1k5	CF		21801
R735	6k8	CF		21807
R736	470	CF		21797
R737	150k	MF	2	38646
R738	10k	CF		21809
R739	3k3	CF		21803
R740	1k5	CF		21801
R741	270k	CF		32356
R742	8k2	CF		21808
R743	10k	CF		21809
R744	10k	CF		21809
R745	220k	MF	2	38650
R746	15k	CF		28727
R747	15k	CF		28727
R748	470	CF		21797
R749	510	MF	2	38587
R750	10	CF		21793
R751	560	CF		21798
R752	220	CF		21796
R753	1k5	CF		21801
R754	1k5	CF		21801

Ref	Value	Description	Tol % ±	Part No
RESISTORS (Cont)				
R755	8k2	CF		21808
R756	12k	CF		21810
R757	33k	CF		21814
R758	470k	CF		32330
R759	470k	CF		32330
R760	22k	CF		21812
R761	5k	PCP		39234
R762	10k	CF		21809
R763	56	CF		28715
R764	68k	CF		21816
R765	18k	MF	2	38624
R766	9k1	MF	2	38617
R767	50k	PCP		39268
R768	5k6	CF		21806
R769	39k	CF		28728
R770	2k7	CF		28726
R771	910	MF	2	38593
R772	2k7	CF		28726
R773	390	CF		28722
R774	47	CF		28714
R775	47	CF		28714
R776	47	CF		28714
R777	15	CF		
R778	10k	CF		21809
R779	1k2	CF		21800
R780	39k	CF		28728
R781				
R782	390	CF		28722
R783	3k9	CF		21804
R784	1k	CF		21799
R785	470	CF		21797
R786	680	CF		28723
R787	2k7	CF		28726
R788	8k2	CF		21808
R789	1k	CF		21799
R790	2k2	CF		21802
R791	3k9	CF		21804
R792	470	CF		21797
R793	220	CF		21796
R794	39	CF		28713
R795	470	CF		21797
R796	10k	CF		21809
R797				
R798	15	CF		28708
R799	1k	CF		21799
R800	1k	CF		21799
R801	390	CF		28722
R802	360	MF	2	38583
R803	6k8	CF		21807
R804	820	MF	2	38592
R805	10	CF		21793
R806	2k7	CF		28726
R807	10	CF		21793
R808	1k8	CF		28725
R809	510	MF	2	38587

OS3500 TIMEBASE (Cont)

Ref	*Value*	*Description*	*Tol %±*	*Part No*	*Ref*	*Value*	*Description*	*Tol %±*	*Part No*
RESISTORS (Cont)					**RESISTORS (Cont)**				
R810	560	CF		21798	R871	6k8	CF		21807
R811	15k	CF		28727	R872	6k8	CF		21807
R812	1k5	CF		21801	R873	4k7	CF		21805
R813	10k	CF		21809	R874	12k	CF		21810
R814	8k2	CF		21808					
R815	22k	CF		21812	R880	6k8	CF		21807
R816	5k	PCP		39234	R881	220	CF		21796
R817	8k2	CF		21808	R882	100	CF		21794
R818	15k	CF		28727	R883	5k6	MF	2	38612
R819	220	CF		21796	R884	5k6	MF	2	38612
R820	4R7	CF		29433	R885	100	CF		21794
R821	12k	CF		21810	R886	5k6	CF		21806
R822	470k	CF		32330	R887	47k	CF		21815
R823	470k	CF		32330	R888	47k	CF		21815
R824	33k	CF		21814					
R825	3k3	CF		21803	R890	3k9	CF		21804
R826	470	CF		21797	R891	470	CF		21797
R827	430	MF	2	38525	R892				
R828	100	CF		21794	R893	3k3	CF		21803
R829	56	CF		28715	R894	390	CF		28722
R830	68k	CF		21816	R895	390	CF		28722
R831	39k	CF		28728	R896	560	CF		21798
R832	9k1	MF	2	38617	R897	47	CF		28714
R833	50k	PCP		39268	R898	47	CF		28714
R834	18k	MF	2	38624	R899	47k	CF		21815
R835	5k6	CF		21806	R900	10	CF		21793
R836	1k2	CF		21800	R901	4k7	CF		21805
R837	47	CF		28714	R902	1k	CF		21798
R838	1k5	CF		21801	R903	4k7	CF		21805
R839	39k	CF		28728	R904	4k7	CF		21805
R840	4k7	CF		21805	R905	4k7	CF		21805
R841	5k6	CF		21806	R906	10	CF		21793
R842	10k	CF		21809	R907	6k8	CF		21807
					R908	6k8	CF		21807
R850	10k	PCP		39265	R909	56k	CF		28729
R851	4k3	MF	2	38609	R910	4k7	CF		21805
R852	5k6	CF		21806	R911	2k2	CF		21802
R853	3k9	CF		21804	R912				
R854	2k2	CF		21802	R913	100	CF		21794
R855	10k	CF		21809	R914	100	CF		21794
R856	2k2	CF		21802	R915	1k	PCP		39233
R857	2k2	CF		21802	R916	910	MF		38593
R858	2k2	CF		21802	R917	100	CF		21794
R859	1k5	CF		21801	R918				
R860	1k5	CF		21801	R919	4k7	CF		21805
R861	4k7	CF		21805					
R862	4k7	CF		21805	R928	100	CF		21794
R863	4k7	CF		21805	R929	22	CF		28710
R864	4k7	CF		21805	R930	1k2	CF		21800
R865	6k8	CF		21807	R931	680	CF		28723
R866	6k8	CF		21807	R932	47	CF		28714
R867	4k7	CF		21805	R933	220	CF		21796
R868	6k8	CF		21807	R934	220	CF		21796
R869	4k7	CF		21805	R935	100	CF		21794
R870	6k8	CF		21807	R936	100	CF		21794

OS3500 TIMEBASE (Cont)

Ref	Value	Description	Tol % ±		Part No
RESISTORS (Cont)					
R937	47k	MF	2	½W	28814
R938	47k	MF	2	½W	28814
R939	68	CF			28716
R940	680	CF			28723
R941	330	CF			28721
R942	560	CF			21798
R943	68	CF			28716
R944	47k	MF	2	½W	28814
R945	10	CF			21793
R946	470	CF			21797
R947	47	CF			28714
R948	6k8	CF			21807
R949	6k8	CF			21807
R950	10	CF			21793
R951	43k	MF	2		38633
R952	82k	MF	2		38640
R953	22	CF			28710
R954	12k	MF	2		38620
R955	12k	MF	2		38620
R956	470	CF			21797
R957	1k	PCP			39233
R958	220	CF			21796
R959	220	CF			21796
R960	10k	PCP			39265
R961	5k6	CF			21806
R962	2k2	MF	2		38602
R963	2k2	MF	2		38602
R964	4k7	CF			21805
R965	2k2	CF			21802
R966	56k	CF			28729
R967	5k6	CF			21806
R968	36k	MF	2		39631
R969	1k6	MF	2		38599
R970	12k	MF	2		38620
R971	12k	CF	A.O.T.		21810
R972	5k6	CF	A.O.T.		21806
R973	750	MF	2		38591
R974	5k6	MF	2		38612
R975	11k	MF	2		38619
R976	30k	MF	2		38629
R977	10	CF			21793
R978	3k9	CF			21804
R979	22	CF			28710
R980	220	CF			21796
R981	220	CF		½W	21796
R982	680	CF			28723
R983	9k1	MF	2		38617
R984	3k3	CF			21803
R985	10k1	MF			37778
R986					
R987	1k3	MF	2		38597

CAPACITORS

C700

Ref	Value	Description		Tol % ±	Part No
CAPACITORS (Cont)					
C701	1nF	CE(2)			22387
C702	10nF	E	+40 -20	250V	22395
C703	10µF	CE(2)		10V	40353
C704	10nF	CE(2)	+40 -20	250V	22395
C705	10nF	CE(2)	+40 -20	250V	22395
C706	33pF	CE(2)		250V	22370
C707	10nF	CE(2)	+40 -20	250V	22395
C708	10nF	CE(2)	+40 -20	250V	22395
C709	1µF	T		35V	54221
C710	47pF	CE(2)			22372
C711	10nF	CE(2)	+40 -20	250V	22395
C712	1µF	PE		100V	37389
C713	10nF	PE		100V	39190
C714	10µF	E		10V	40353
C715	220pF	CE(2)			22379
C716	56pF	CE(2)			22373
C717	100nF	PE		100V	37018
C718	68pF	CE(2)			22374
C719	2µF2	PC	5	160V	40853
C720	22nF	PC	2	160V	40854
C721	180pF	SM	1	350V	4515
C722	45pF	TRIMMER			36274
C723	10nF	CE(2)	+40 -20	250V	22395
C724	10µF	E		25V	32180
C725					
C726	10nF	CE(2)	+40 -20	250V	22395
C727					
C728					
C729	10nF	CE(2)	+40 -20	250V	22395
C730	10nF	CE(2)	+40 -20	250V	22395
C731	10nF	CE(2)	+40 -20	250V	22395
C732	10nF	CE(2)	+40 -20	250V	22395
C733	10nF	CE(2)	+40 -20	250V	22395
C734	10nF	CE(2)	+40 -20	250V	22395
C735	68pF	CE(2)			22374
C736	10nF	CE(2)	+40 -20	250V	22395
C737	10nF	CE(2)	+40 -20	250V	22395
C738	10nF	CE(2)	+40 -20	250V	22395

OS3500 TIMEBASE (Cont)

Ref	Value	Description	Tol % ±		Part No
CAPACITORS (Cont)					
C739	56pF	CE(2)			22373
C740	180pF	SM	1	350V	4515
C741	45pF	TRIMMER			36274
C742	2μF2	PC	5	160V	40853
C743	10μF	E		10V	40353
C744	10μF	E		25V	32180
C745	10nF	CE(2)	+40 -20	250V	22395
C746	22nF	PC	2	160V	40854
C747	220pF	CE(2)			22379
C748	10nF	CE(2)	+40 -20	250V	22395
C749	56pF	CE(2)			22373
C750	10nF	CE(2)	+40 -20	250V	22395
C751	10μF	E		25V	32180
C752	10nF	CE(2)	+40 -20	250V	22395
C753	100nF	PE		100V	37018
C754			A.O.T.		
C755			A.O.T.		
C756	10μF	E		10V	40353
C757	10nF	CE(2)	+40 -20	250V	22395
C758	56pF	CE(2)			22373
C759	10nF	CE(2)	+40 -20	250V	22395
C760	10nF	CE(2)	+40 -20	250V	22395
C761	1μF	T		35V	54221
C762	1μF	T		35V	54221
C763	100pF	CE(2)			22376
C764	10nF	CE(2)	+40 -20	250V	22395
C765	10nF	CE(2)	+40 -20	250V	22395
C766	10μF	E		25V	32180
C767	10nF	CE(2)	+40 -20	250V	22395
C768	10nF	CE(2)	+40 -20	250V	22395
C769	10nF	CE(2)	+40 -20	250V	22395
C770	10nF	CE(2)	+40 -20	250V	22395
C771	10nF	CE(2)	+40 -20	250V	22395
C772	10μF	E		25V	32180
C773	27pF	CE(2)			22369
C774	10nF	CE(2)	+40 -20	250V	22395
C775	680pF	CE(2)			22385
C776	22μF	T		16V	54220
C777	10nF	CE(2)	+40 -20	250V	22395

Ref	Value	Description	Tol % ±		Part No
CAPACITORS (Cont)					
C801	10nF	CE(2)		250V	22395
C802	10nF	CE(2)		250V	22395
C803	10nF	CE(2)		250V	22395
C804	10nF	CE(2)		250V	22395
C805	10nF	CE(2)		250V	22395
C806	10nF	CE(2)		250V	22395
C807	10nF	CE(2)		250V	22395
C808	10nF	CE(2)		250V	22395
C809	10nF	CE(2)		250V	22395
C810	2pF2	S.M.	½pF	350V	815
C811	2pF2	S.M.	½pF	350V	815
C812	10nF	CE(2)	+40 -20	250V	22395
C813	1pF5	CE(2)	¼pF		40356
C814	1pF5	CE(2)	¼pF		40356
C815	9pF	TRIMMER			36272
C816	9pF	TRIMMER			36272
C817	1pF	CE(2)	¼pF		40357
C818	1pF	CE(2)	¼pF		40357
C819	100nF	PE		100V	37018
C820	150pF	CE(2)			22378
C821	150pF	CE(2)			22378
C822	10nF	CE(2)	+40 -20	250V	22395
C823	10nF	CE(2)	+40 -20	250V	22395
C824	10nF	CE(2)	+40 -20	250V	22395
C825	10μF	E		15V	32180
C826	10nF	CE(2)		250V	22395
C827	10nF	CE(2)		250V	22395
C828	10nF	CE(2)		250V	22395
C829	10nF	PE		100V	37018
C830	470pF	CE(2)			22383
C831	33pF	CE(2)			22370
C841	10μF	E		25V	32180
C842	33μF	E		16V	32173
C843	33μF	E		16V	32173
C844	150nF	PE		250V	35601
C845	39pF	CE(2)			22371

OS3500 TIMEBASE (Cont)

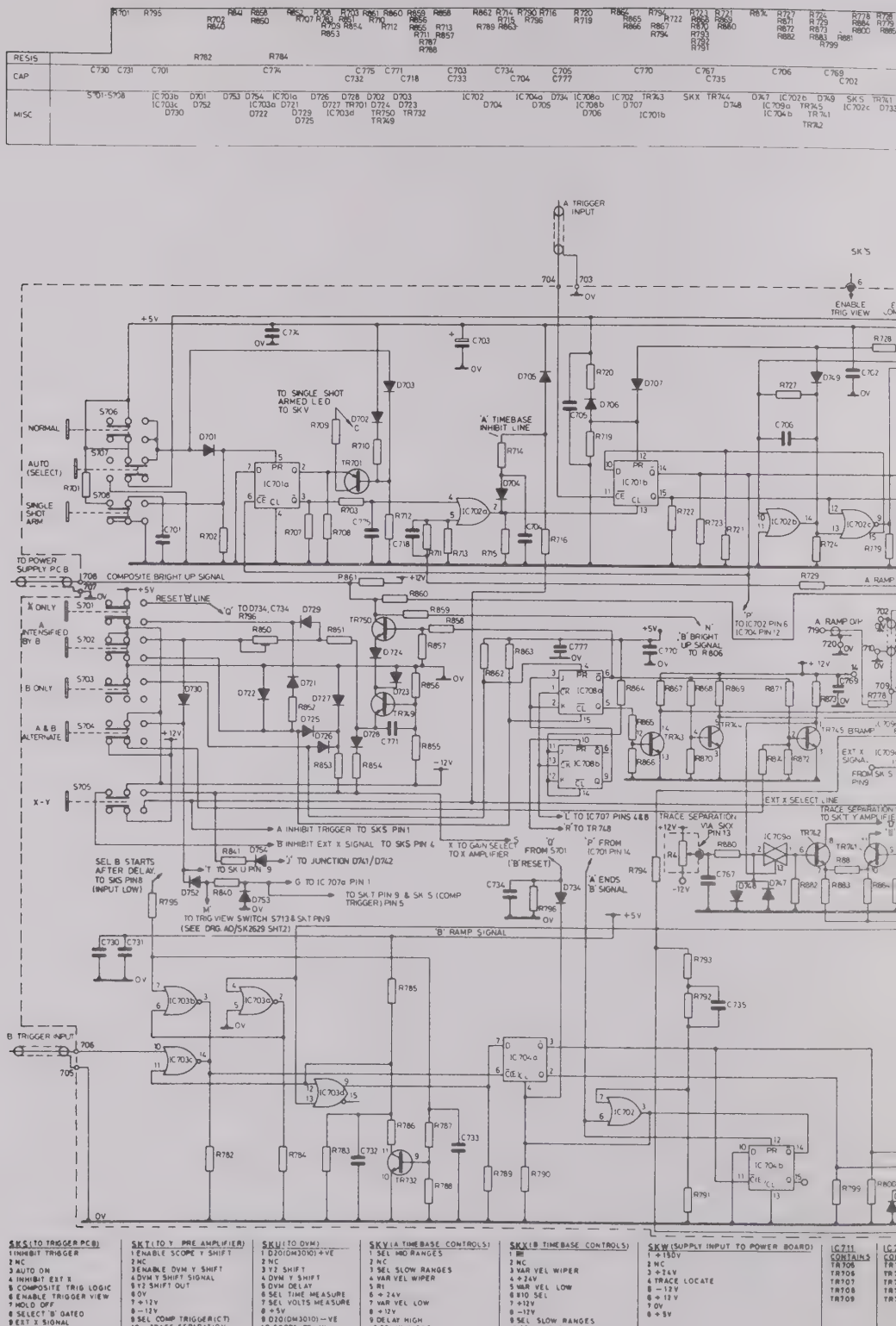
Ref	Value	Description	Tol %±	Part No
TRANSISTORS				
TR701		BC212		29327
TR702		2N5771		38089
TR703		2N3906		21533
TR704		2N5771		38089
TR705		PART OF IC711		
TR706				
TR707		PART OF IC711		
TR708				
TR709				
TR710		BC182B NATIONAL OR TEXAS ONLY		40349
TR711		2N5771		38089
TR712		BC214C		36019
TR713		2N3904		24146
TR714		BC214C NATIONAL OR TEXAS ONLY		40348
TR715		BC182B		33205
TR716		BC212		29327
TR717		DUAL FET WD406		A36306
TR718				
TR719		MPS2369		36625
TR720		MPS2369		36625
TR721		2N3904		24146
TR722		ZTX3906		41811
TR723		ZTX3906		41811
TR724		2N5771		38089
TR725		2N5771		38089
TR726		2N3906		21533
TR727		BC182B NATIONAL OR TEXAS ONLY		40348
TR733		2N3640		31781
TR734		2N3904		24146
TR735		2N3904		24146
TR736		DUAL FET WD406		A36306
TR737				
TR738		BC214C NATIONAL OR TEXAS ONLY		40348
TR739		BC182B		33205
TR740		BC212		29327
TR741		PART OF IC712		
TR742				
TR743				
TR744				
TR745				
TR746		MPS2369		36625
TR747		MPS2369		36625
TR748		2N3904		24146
TR749		2N3904		24146
TR750		2N3904		24146
TR751		BC212		29327
TR801		BF470		38416
TR802		BF470		38416

Ref	Value	Description	Tol %±	Part No
TRANSISTORS (Cont)				
TR803		BF469		38418
TR804		BF469		38418
TR805		2N5771		38089
TR806		2N2369		23307
TR807		2N5771		23307
TR808		BF371		38089
TR809		BF371		36275
TR810		BF371		36275
TR811		BF371		36275
TR812		2N3904		36275
TR813		2N3904		24146
TR814		2N3904		24146
TR815		2N3904		24146
DIODES				
D700				
D701		IN4148		23802
D702		IN4148		23802
D703		IN4148		23802
D704		IN4148		23802
D705		IN4148		23802
D706		IN4148		23802
D707		IN4148		23802
D708		IN4148		23802
D709		IN4148		23802
D710		IN4148		23802
D711		IN4148		23802
D712	3.9V	BZX79 ZENER	5	33925
D713		IN4148		23802
D714		IN4148		23802
D715		IN4148		23802
D716		IN4148		23802
D717		IN4148		23802
D718		IN4148		23802
D719		IN4148		23802
D720	2.7V	BZX79 ZENER	5	33921
D721		IN4148		23802
D722		IN4148		23802
D723		IN4148		23802
D724		IN4148		23802
D725		IN4148		23802
D726		IN4148		23802
D727		IN4148		23802
D728		IN4148		23802
D729		IN4148		23802
D730		IN4148		23802
D731	3.9V	BZX79 ZENER	5	33925
D732		IN4148		23802
D733		IN4148		23802
D734		IN4148		23802
D735		IN4148		23802
D736		IN4148		23802
D737		IN4148		23802
D738		IN4148		23802
D739		IN4148		23802

OS3500 TIMEBASE (Cont)

Ref	*Value*	*Description*	*Tol %±*	*Part No*
DIODES (Cont)				
D740	5V6	ZENER BZX79	5	33929
D741		IN4148		23802
D742		IN4148		23802
D743		OA 47		4468
D744		IN4148		23802
D745		IN4148		23802
D746		IN4148		23802
D747		IN4148		23802
D748		IN4148		23802
D749		IN4148		23802
D750		IN4148		23802
D751		IN4148		23802
D752		IN4148		23802
D753		IN4148		23802
D754		IN4148		23802
D801	5.6V	ZENER BZX79	5	33929
D802	3.9V	ZENER BZX79	5	33925
D803	7.5V	ZENER BZX79	5	33932
D804		IN4149		1949
D805		IN4149		1949
D806		IN4149		1949
D807		IN4149		1949
D808		FH1100		40352
D809		FH1100		40352
D810		IN4149		1949
D811		IN4149		1949
D812		IN4148		23802
D813		IN4148		23802
D821		IN4148		23802
D822		IN4148		23802

Ref	*Value*	*Description*	*Tol %±*	*Part No*
INTEGRATED CIRCUITS				
IC701		10131		39246
IC702		10103		40346
IC703		10102		39243
IC704		10131		39246
IC705		74LS112		36468
IC706		741		36736
IC707		74L10		32698
IC708		74LS112		36468
IC709		CD4066		40345
IC710		1414		35682
IC711		CA3086		42907
IC712		CA3086		42907
IC713		CA3086		42907
IC714		709		40179
MISCELLANEOUS				
L701		Bead Ferrite FX1242		26986
L702		Bead Ferrite FX1242		26986
S701–705		Switch Assy Pushbutton		40735
S706–708		Switch Assy Pushbutton		40736
S709–713		Switch Assy Pushbutton		41487
SKS		13 Way		39387
SKT		18 Way		40017
SKU		11 Way		40323
SKV		13 Way		39387
SKW		8 Way		37877
SKX		13 Way		39387


A TRIGGER INPUT
SK'S
ENABLE TRIG VIEW
NORMAL
AUTO (SELECT)
SINGLE SHOT ARM
TO SINGLE SHOT ARMED LED TO SK V
'A' TIMEBASE INHIBIT LINE
TO POWER SUPPLY P.C.B
COMPOSITE BRIGHT UP SIGNAL
X ONLY
A INTENSIFIED BY B
B ONLY
A & B ALTERNATE
X-Y
RESET 'B' LINE
'B' BRIGHT UP SIGNAL TO R806
A RAMP O/P
A INHIBIT TRIGGER TO SK5 PIN 1
'B' INHIBIT EXT X SIGNAL TO SK5 PIN 4
'J' TO JUNCTION D741/D742
'T' TO SK U PIN 9
G TO IC 707a PIN 1
TO SK T PIN 9 & SK S (COMP TRIGGER) PIN 5
TO TRG VIEW SWITCH S713 & SK T PIN 9
(SEE DRG AO/SK2629 SHT2)
SEL B STARTS AFTER DELAY TO SK5 PIN 8 (INPUT LOW)
'B' RAMP SIGNAL
B TRIGGER INPUT
EXT X SELECT LINE
TRACE SEPARATION VIA SK X PIN 13
TRACE SEPARATION TO SK T Y AMPLIFIER
'A' ENDS 'B' SIGNAL
'B' RESET
FROM S701
FROM IC 701 PIN 14
X TO GAIN SELECT TO X AMPLIFIER
L TO IC 707 PINS 4&8
R TO TR 748
EXT X SIGNAL FROM SK S PIN 9

SKS (TO TRIGGER P.C.B)
1 INHIBIT TRIGGER
2 NC
3 AUTO ON
4 INHIBIT EXT X
5 COMPOSITE TRIG LOGIC
6 ENABLE TRIGGER VIEW
7 HOLD OFF
8 SELECT 'B' GATED
9 EXT X SIGNAL
10 0V
11 +8V
12 +12V
13 −12V

SKT (TO Y PRE AMPLIFIER)
1 ENABLE SCOPE Y SHIFT
2 NC
3 ENABLE DVM Y SHIFT
4 DVM Y SHIFT SIGNAL
5 Y2 SHIFT OUT
6 0V
7 +12V
8 −12V
9 SEL COMP TRIGGER (CT)
10 TRACE SEPARATION
11 SIGNAL
12 SEL CHOP (CH)
13 SEL TRIG VIEW (TV)
14 SEL CH 1 (C1)
15 +8V
16 SEL SUM (S)
17 SEL CH2 (C2)
18 CHANNEL SWITCH PHASE

SKU (TO DVM)
1 D20 (OR 3010) +VE
2 NC
3 Y2 SHIFT
4 DVM Y SHIFT
5 DVM DELAY
6 SEL TIME MEASURE
7 SEL VOLTS MEASURE
8 +5V
9 D20 (OR 3010) −VE
10 SCOPE DELAY
11 0V

SKV (A TIMEBASE CONTROLS)
1 SEL MID RANGES
2 NC
3 SEL SLOW RANGES
4 VAR VEL WIPER
5 R1
6 +24V
7 VAR VEL LOW
8 +12V
9 DELAY HIGH
10 DELAY WIPER
11 DELAY LOW
12 D14 (S SHOT) +VE
13 0V

SKW (B TIMEBASE CONTROLS)
1
2 NC
3 VAR VEL WIPER
4 +24V
5 VAR VEL LOW
6 B10 SEL
7 +12V
8 −12V
9 SEL SLOW RANGES
10 SEL MID RANGES
11 COARSE X SHIFT
12 FINE X SHIFT
13 TRACE SEP SHIFT

SKW (SUPPLY INPUT TO POWER BOARD)
1 +190V
2 NC
3 +24V
4 TRACE LOCATE
5 −12V
6 +12V
7 0V
8 +8V

IC711 CONTAINS
IC706
IC706
IC707
IC708
IC709

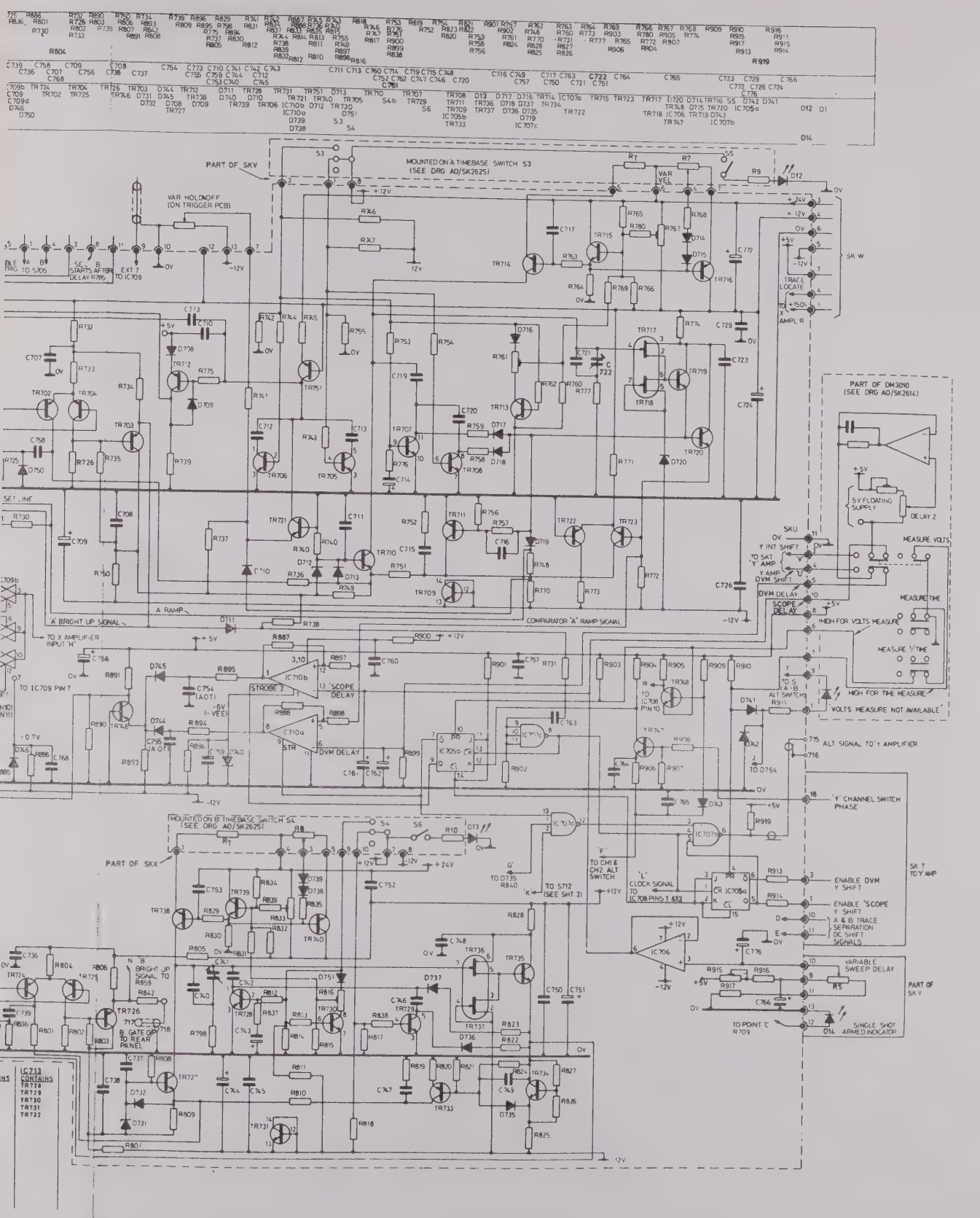

PART OF SKV
MOUNTED ON A TIMEBASE SWITCH S3 (SEE DRG AO/SK2625)
VAR HOLDOFF (ON TRIGGER PCB)
SK W
PART OF DM3010 (SEE DRG AO/SK2614)
5V FLOATING SUPPLY
DELAY 2
MEASURE VOLTS
MEASURE TIME
HIGH FOR VOLTS MEASURE
HIGH FOR TIME MEASURE
VOLTS MEASURE NOT AVAILABLE
A BRIGHT UP SIGNAL
A RAMP
COMPARATOR 'A' RAMP SIGNAL
SET LINE
TO X AMPLIFIER INPUT 'H'
STROBE 2
'SCOPE DELAY'
DVM DELAY
ALT SIGNAL TO 'Y' AMPLIFIER
'Y' CHANNEL SWITCH PHASE
MOUNTED ON B TIMEBASE SWITCH S4 (SEE DRG AO/SK2625)
PART OF SKX
TO CH1 & CH2 ALT SWITCH
CLOCK SIGNAL TO IC708 PINS 1 &13
ENABLE DVM Y SHIFT
ENABLE 'SCOPE Y SHIFT
A & B TRACE SEPARATION DC SHIFT SIGNALS
VARIABLE SWEEP DELAY
PART OF SK V
SINGLE SHOT ARMED INDICATOR
B GATE OUT TO REAR PANEL
IC713 CONTAINS TR728 TR729 TR730 TR731 TR732

Fig. 9 Circuit Diagrams Timebase

| | | |

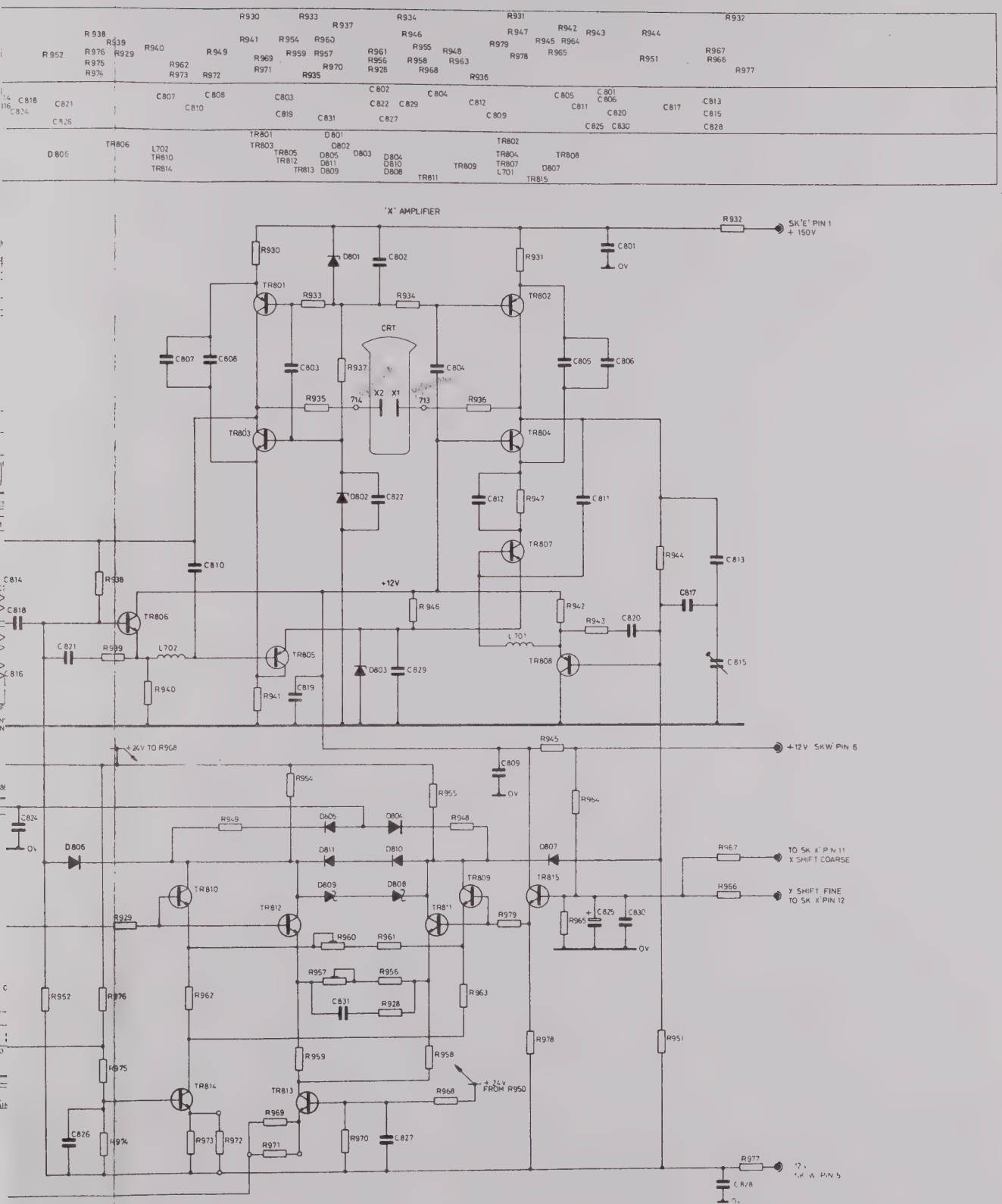


Fig. 10 Circuit Diagrams 'X' Output Amplifier

OS3500 POWER SUPPLY

Ref	Value	Description	Tol % ±		Part No
RESISTORS					
R1001	2k2	CF			21802
R1002	39	CF			28713
R1003	4k7	MF	2		38610
R1004					
R1005	1k2	MF	2		38596
R1006					
R1007	10	CF			21793
R1008	2k2	MF	2		38602
R1009	1k5	CF			21801
R1010					
R1011	47	CF			28714
R1012	18k	CF			21811
R1013	5k6	CF			21806
R1014	5k6	MF	2		38612
R1015					
R1016	33k	CF			21814
R1017	100	CF			21794
R1018	100	CF			21794
R1019	30k	MF	2		38629
R1020					
R1021	100	CF			21794
R1022	47k	CF			21815
R1023	68k	CF			21816
R1024	10k	CF			21809
R1025	1k6	MF	2		38599
R1026	100	CF			21794
R1027	2k7	WW	5	2½W	40370
R1028					
R1029	6k8	MF	2		38614
R1030					
R1031					
R1032	3k3	CF			21803
R1033	10	CF			21793
R1034		CF			
R1035	82k				21818
R1036	56k	CF			28729
R1037	120k	CF			21820
R1038	39k	CF			28728
R1039	1M	CF			31840
R1040					
R1041	15	CF		1W	19026
R1042	2k7	MF	2	½W	26728
R1043	200	MF	2		38577
R1044	2k	MF	2		38601
R1045					
R1046					
R1047	200	MF	2		38577
R1048	2k	MF	2		38601
R1049	243	MF	1		36628
R1050	750	MF	1		40369
R1051	100	PCP			39230
R1052	100	PCP			39230
R1053	1k5	CF			21801
R1054	5k6	CF	A.O.T.		21806
R1055	3k57		1		42962

Ref	Value	Description	Tol % ±	Part No
RESISTORS (Cont)				
R1056	21k5		1	42961
R1101	100	CF		21794
R1102	820	CF		28724
R1103	68k	CF		21816
R1104				
R1105	22k	CF		21812
R1106	50k	PCP		39268
R1107	1k	CF		21799
R1108				
R1109	5k6	CF		21806
R1110				
R1111	1k5	CF		21801
R1112	220	CF		21796
R1113	1k	CF		21799
R1114	27k	CF		21813
R1115				
R1116				
R1117	100	CF		21794
R1118	10k	CF		21809
R1119	1M	PCP		39268
R1120	10k	CF		21809
R1121	15M	MG		40371
R1122				
R1123	10k	CF		21809
R1124	1M5	CF		40729
R1125	15M	MG		40371
CAPACITORS				
C1	1000µF	E	100V	A4/40765
C2	6800µF	E	25V	A4/40766
C3	6800µF	E	25V	A4/40766
C1001	.01µF	CE(2)	250V	22395
C1002	.01µF	CE(2)	250V	22395
C1003	56pF	CE(2)	500V	22373
C1004	.01µF	CE(2)	250V	22395
C1005	.01µF	CE(2)	250V	22395
C1006	22µF	E	25V	32181
C1007	.01µF	CE(2)	250V	22395
C1008	.1µF	PE	100V	37018
C1009	22µF	E	25V	32181
C1010	100pF	CE(2)	500V	22376
C1011	.01µF	CE(2)	250V	22395
C1012	.01µF	CE(2)	250V	22395
C1013	4700pF	CE(2)	500V	22393
C1014	3000pF	CE(1)	3kV	34381
C1015	.01µF	PE	2kV	32066
C1016	220µF	E	16V	42757
C1017	470µF	E	63V	40586
C1018				
C1019	220µF	E	100V	40587
C1020				
C1021	220µF	E	100V	40587

OS3500 POWER SUPPLY (Cont)

Ref	Value	Description	Tol %±	Part No
CAPACITORS (Cont)				
C1022	22µF	E	25V	32181
C1023	22µF	E	25V	32181
C1024				
C1025	6800µF	E	16V	A4/40559
C1026	22µF	E	25V	32181
C1027	4.7µF	T	25V	53249
C1028	4.7µF	T	25V	53249
C1101				
C1102	22µF	E	25V	32181
C1103	150pF	CE(2)	500V	22378
C1104	.1µF	PE	100V	37018
C1105	.1µF	PS	250V	39199
C1106	68µF	T	16V	40560
C1107				
C1108				
C1109	470pF	CE(1)	2kV	40561
C1110				
C1111	470pF	CE(1)	2kV	40561
C1112	.01µF	CE(2)	250V	22395
C1113				
C1114	4700pF	CE(1)	4kV	40562
C1115	4700pF	CE(1)	4kV	40562
C1116	4700pF	CE(1)	4kV	40562

Ref	Value	Description	Part No
TRANSISTORS			
TR1001		BC212	29327
TR1002		2N5771	38089
TR1003		BC449	40129
TR1005		BC182B	33205
DIODES			
D1		IN4003	32771
D2		IN4003	32771
D3		IN4003	32771
D4		IN4003	32771
D5		IN4003	32771
D6		IN4003	32771
D7		IN4003	32771
D8		IN4003	32771
D9		IN4003	32771
D10		IN4003	32771
D1006		IN4148	23802
D1007		IN4148	23802
D1008	18V	ZENER	33941
D1009			
D1010		IN4003	32771
D1011		IN4003	32771
D1012		IN4003	32771
D1013		IN4003	32771

Ref	Value	Description	Part No
DIODES (Cont)			
D1016	47V	ZENER	40049
D1017		IN4003	32771
D1018		IN4003	32771
D1021		IN4003	32771
D1022		IN4003	32771
D1023		IN4003	32771
D1024			
D1025		IS922	40821
D1101		IN4148	23802
D1102		IN4148	23802
D1103		IN4148	23802
D1104		IN4148	23802
D1105		IN4148	23802
D1106			
D1107		ED1	35278
D1108		ED1	35278
D1109		IN4148	23802
D1110			
D1111		ED1	35278
D1112		ED1	35278
D1113			
D1114		IN5271	37557
INTEGRATED CIRCUITS			
IC1001		LM317	40731
IC1002		LM317	40731
IC1003		LM317	40731
IC1004		µA723	31228
MISCELLANEOUS			
BR1001		WO2	19725
BR1002		WO2	19725
L1		TWIST COIL	A3/35997
L1101	150µH		40564
T1			A1/37931
T1101			A2/40094
S1			A4/36232
S15			4069
S16			4069
FS1	500mA	240V SUPPLY	33685
	1A	115V SUPPLY	34790
FS1001	500mA	SLO-BLO	33685
MPR1		EHT MULTIPLIER	40588

1400 _ 6 IRONSIDE DR
SANTA CLARA CALIF
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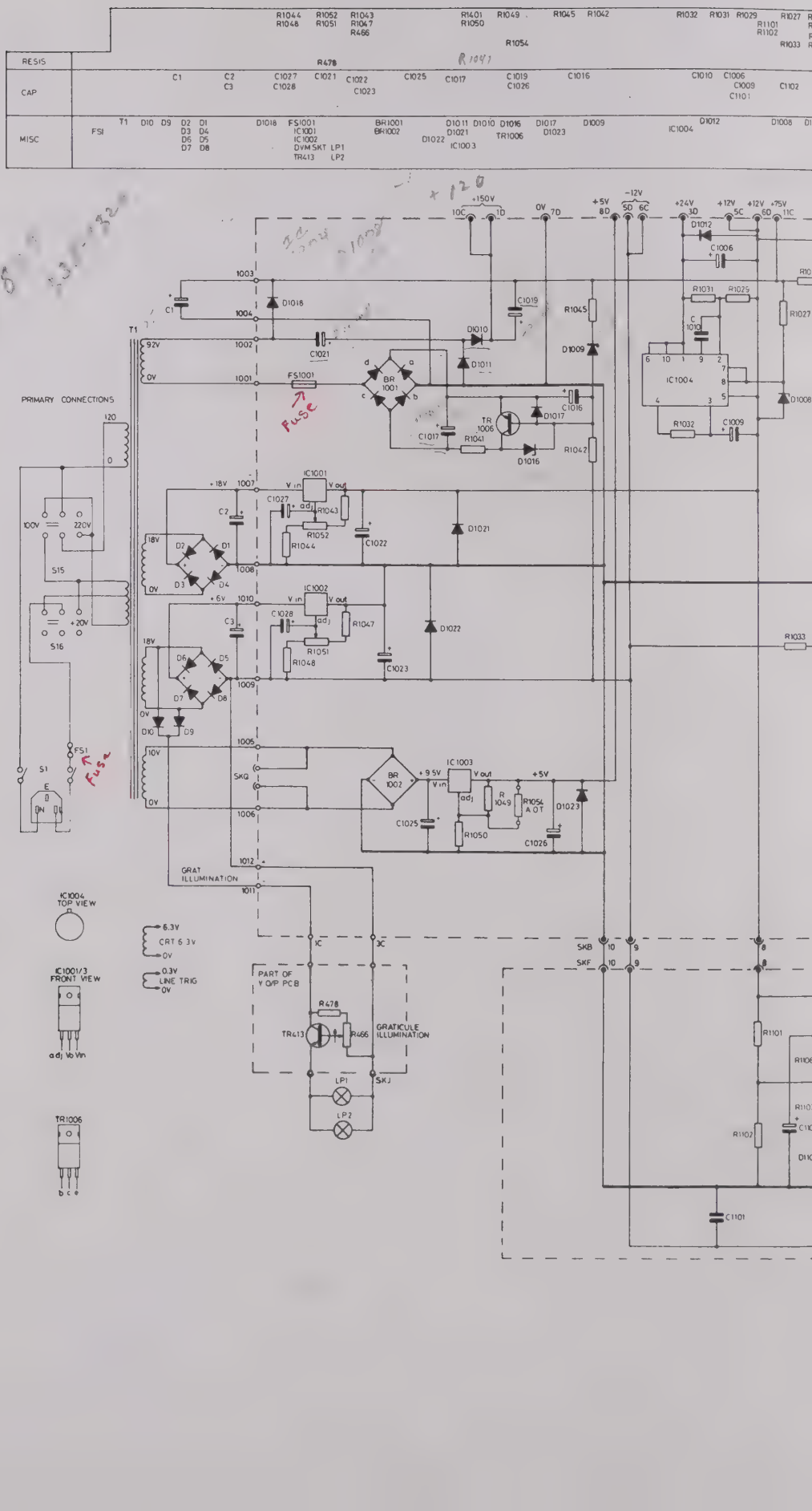

RESIS
CAP
MISC
R478
R1041
R1054
C1
C2
C3
C1027
C1028
C1021
C1022
C1023
C1025
C1017
C1019
C1026
C1016
C1010
C1006
C1009
C1101
C1102
R1044
R1048
R1052
R1051
R1043
R1047
R466
R1401
R1050
R1049
R1045
R1042
R1032
R1031
R1029
R1101
R1102
R1027
R1033
T1
FSI
D10
D9
D2
D3
D6
D7
D1
D4
D5
D8
D1018
FS1001
IC1001
IC1002
DVM SKT
TR413
LP1
LP2
BR1001
BR1002
D1022
D1011
D1021
IC1003
D1010
D1016
TR1006
D1017
D1009
D1012
IC1004
D1008
+150V
0V
+5V
-12V
+24V
+12V
+12V
+75V
10C
1D
7D
8D
5D
6C
1D
5C
6D
11C
1003
1004
1002
1001
92V
0V
PRIMARY CONNECTIONS
120
0
100V
220V
S15
+20V
S16
S1
E
IN
FS1
Fuse
Fuse
IC1001
V in
V out
adj
+18V
18V
0V
1007
1008
D1
D2
D3
D4
IC1002
+6V
1010
1009
D5
D6
D7
D8
D9
D10
1005
10V
SKQ
1006
IC1003
BR 1002
+9.5V
+5V
R1054 A.O.T.
1012
1011
GRAT ILLUMINATION
IC1004 TOP VIEW
IC1001/3 FRONT VIEW
adj Vo Vin
TR1006
b c e
6.3V
CRT 6.3V
0V
0.3V
LINE TRIG
0V
1C
3C
PART OF Y O/P PCB
R478
TR413
R466
GRATICULE ILLUMINATION
LP1
LP2
SKJ
SKB
SKF
10
9
8
R1101
R1102
C1101

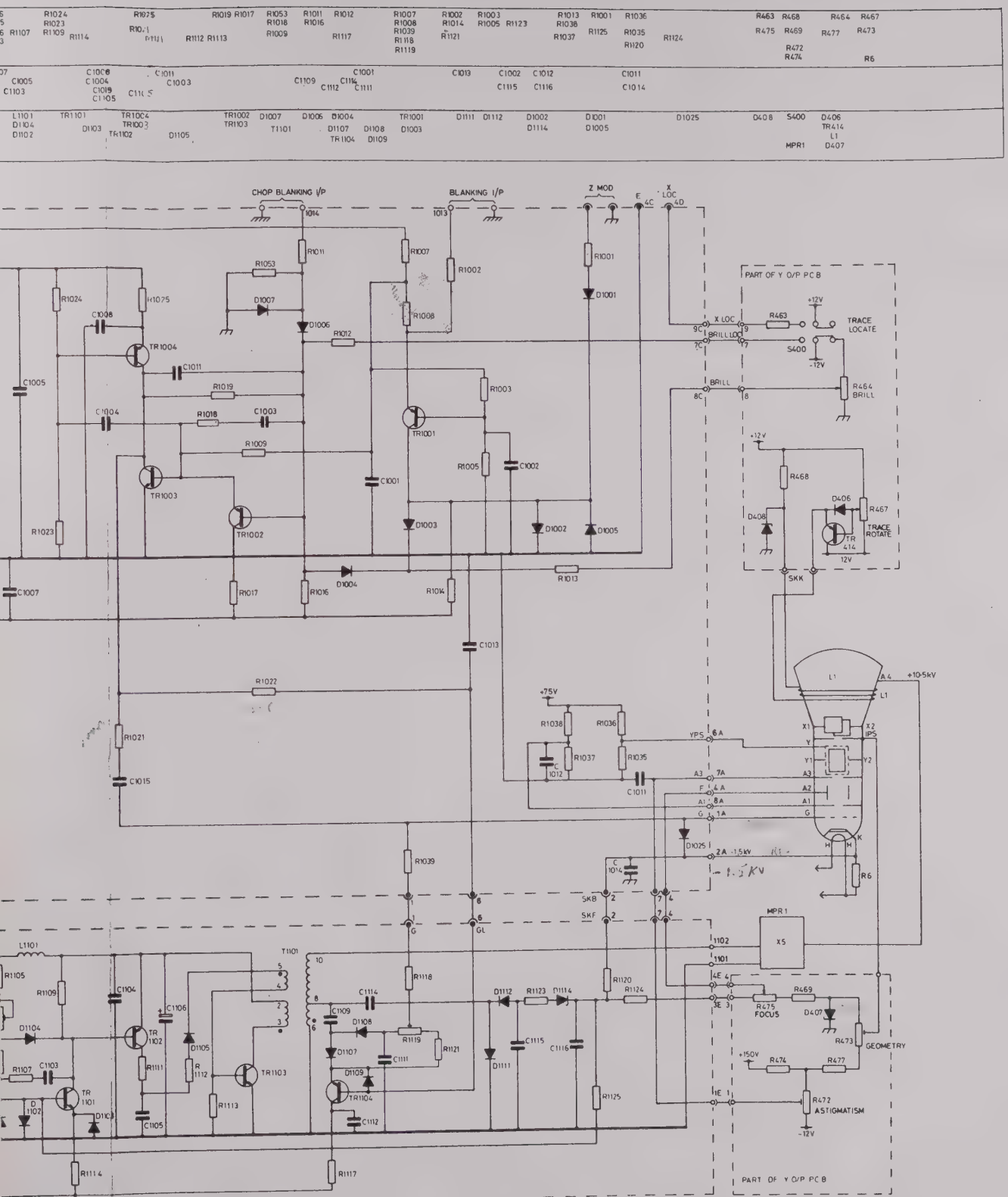


Fig. 11 Circuit Diagrams Power Supply

OS3500 INTERCONNECTIONS

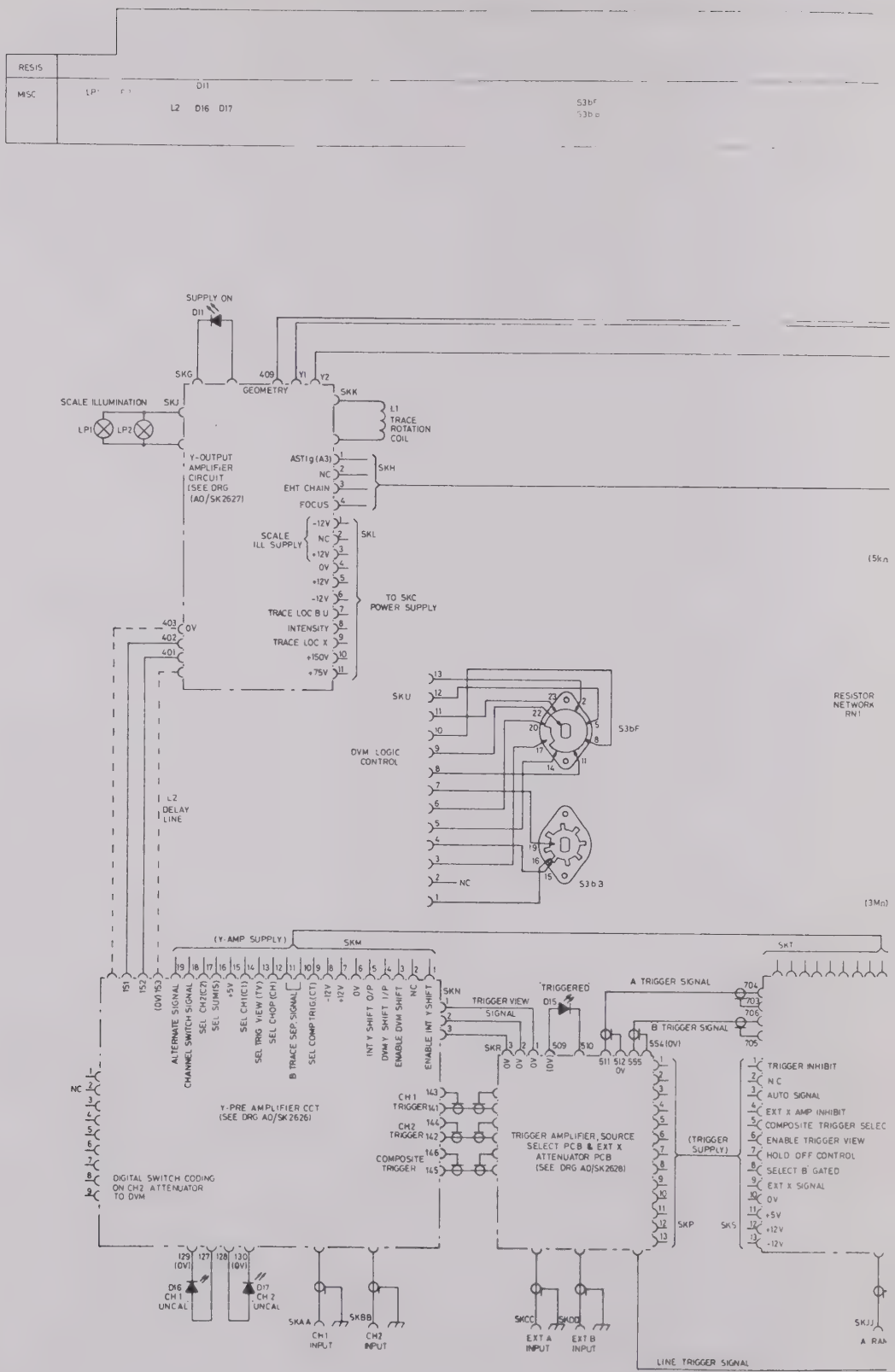
Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R1				
R2	10k	CP	With S2	A4/38689
R3	10k	CP		A4/38689
R4	10k	CP		A4/38673
R5	5k	CP		A4/38685
R6	100k	CF		21819
R7	10k	CP	With S5	A4/38675
R8	10k	CP	With S6	A4/38675
R9	2k2	CF		21802
R10	2k2	CF		21802
R11	1k	CP		A4/42204
R12	4k7	CP		A4/42203
R13	500	CP	With S7	A4/39730 or 43195
R14	500	CP	With S8	A4/38730 or 43195
R15				
R16	10	CF	See Drg. A4/42930	21793
R17	10	CF	See Drg. A4/42930	21793
R51	10	CF		21793
R52	10	CF		21793
R53	10	CF		21793
R54	10	CF		21793
R55	10	CF		21793
R56	10	CF		21793
R57	82	CF		28717
R58	82	CF		28717
R59	100	CF		21794
R60	100	CF		21794
R61	22	CF		28710
R62	22	CF		28710
R63	15	CF		28708
R64	15	CF		28708
R65	22	CF		28710
R66	22	CF		28710
R67	900k	MF Welwyn 4034G	0.5	31929
R68	900k	MF Welwyn 4034G	0.5	31929
R69	100k	MF	2	38642
R70	100k	MF	2	38642
R71	470k	CC		4906
R72	470k	CC		4906
R73	470k	CC		4906
R74	470k	CC		4906
R75	47	CF		28714
R76	47	CF		28714
R77	47	CF		28714
R78	47	CF		28714
R79	900k	MF	0.5 ½W	39129
R80	900k	MF	0.5 ½W	39129
R81	990k	MF	0.5 ½W	39127
R82	990k	MF	0.5 ½W	39127
R83	220	CF		21796

Ref	Value	Description	Tol % ±	Part No
RESISTORS (Cont)				
R84	220	CF		21796
RN1				A4/40102
RN2				A4/40103
RN51				A3/40534
RN52				A3/40534
CAPACITORS				
C51	4.7nF	CE(2)		22393
C52	4.7nF	CE(2)		22393
C53	0.1µF	PE	400V	29495
C54	0.1µF	PE	400V	29495
C55	4.7nF	CE(2)		22393
C56	4.7nF	CE(2)		22393
C57	27pF	CE(2)		22369
C58	27pF	CE(2)		22369
C59	27pF	CE(2)		22369
C60	27pF	CE(2)		22369
C61	47pF	BUTTON MICA		29918
C62	47pF	BUTTON MICA		29918
C63	330pF	BUTTON MICA		31293
C64	330pF	BUTTON MICA		31293
C65	15pF	CE(2)		22366
C66	15pF	CE(2)		22366
C67	3.9pF	SM		34225
C68	3.9pF	SM		34225
C69	10pF	CE(2)		22364
C70	10pF	CE(2)		22364
C71	1.8pF	CE(2)		36597
C72	1.8pF	CE(2)		36597
DIODES				
D11				39884
D12				39884
D13				39884
D14				39884
D15				39884
D16				39884
D17				39884
SWITCHES				
S2			With R2/3	A4/38689
S3				38686
S4				38687
S5			With R7	A4/38675
S6			With R8	A4/38675
S7			With R13	A4/38730 or 43195
S8			With R14	A4/38730 or 43195
S9				41385
S10				40775
S11, S12				A3/40734

OS3500 INTERCONNECTIONS (Cont)

Ref	Value	Description	Tol %±	Part No
SWITCHES (Cont)				
S13 } S14 }				A3/40734
MISCELLANEOUS				
LP1	12V	1W Lamp		40328
LP2	12V	1W Lamp		40328

Ref	Value	Description	Tol %±	Part No
MISCELLANEOUS (Cont)				
L2		Coil c.r.t. twist	40080	
L3		FERRITE BEAD FX1242	26986	U/L/C
L4		FERRITE BEAD FX1242	26986	U/L/C
V1		THORN D14–310GH–82 STANDARD	40080	U/L/C
		THORN D14–310GM–82 LONG PERSISTENCE	40081	U/L/C


RESIS
MISC
D11
L2 D16 D17
SUPPLY ON
D11
SKG
409
GEOMETRY
Y1
Y2
SKK
SCALE ILLUMINATION
SKJ
LP1
LP2
L1
TRACE ROTATION COIL
Y-OUTPUT AMPLIFIER CIRCUIT (SEE DRG (A0/SK2627)
AST1g (A3)
NC
EHT CHAIN
FOCUS
SKH
SCALE ILL SUPPLY
-12V
NC
+12V
0V
+12V
-12V
TRACE LOC B U
INTENSITY
TRACE LOC X
+150V
+75V
SKL
TO SKC POWER SUPPLY
403
402
401
0V
L2 DELAY LINE
SKU
DVM LOGIC CONTROL
S3bF
S3b3
NC
RESISTOR NETWORK RN1
(5kΩ
(3MΩ
(Y-AMP SUPPLY)
SKM
ALTERNATE SIGNAL
CHANNEL SWITCH SIGNAL
SEL CH2(C2)
SEL SUM(S)
+5V
SEL CH1(C1)
SEL TRIG VIEW (TV)
SEL CHOP (CH)
B TRACE SEP. SIGNAL
SEL COMP TRIG(CT)
-12V
+12V
0V
INT Y SHIFT O/P
DVM Y SHIFT I/P
ENABLE DVM SHIFT
NC
ENABLE INT Y SHIFT
SKN
TRIGGER VIEW SIGNAL
TRIGGERED
D15
A TRIGGER SIGNAL
B TRIGGER SIGNAL
554 (0V)
SKR
SKT
Y-PRE AMPLIFIER CCT (SEE DRG A0/SK2626)
CH1 TRIGGER
CH2 TRIGGER
COMPOSITE TRIGGER
TRIGGER AMPLIFIER, SOURCE SELECT PCB & EXT X ATTENUATOR PCB (SEE DRG A0/SK2628)
(TRIGGER SUPPLY)
SKP
SKS
TRIGGER INHIBIT
N C
AUTO SIGNAL
EXT X AMP INHIBIT
COMPOSITE TRIGGER SELEC
ENABLE TRIGGER VIEW
HOLD OFF CONTROL
SELECT B GATED
EXT X SIGNAL
0V
+5V
+12V
-12V
DIGITAL SWITCH CODING ON CH2 ATTENUATOR TO DVM
D16 CH1 UNCAL
D17 CH2 UNCAL
SKAA
CH1 INPUT
SKBB
CH2 INPUT
SKCC
EXT A INPUT
SKDD
EXT B INPUT
SKJJ
LINE TRIGGER SIGNAL

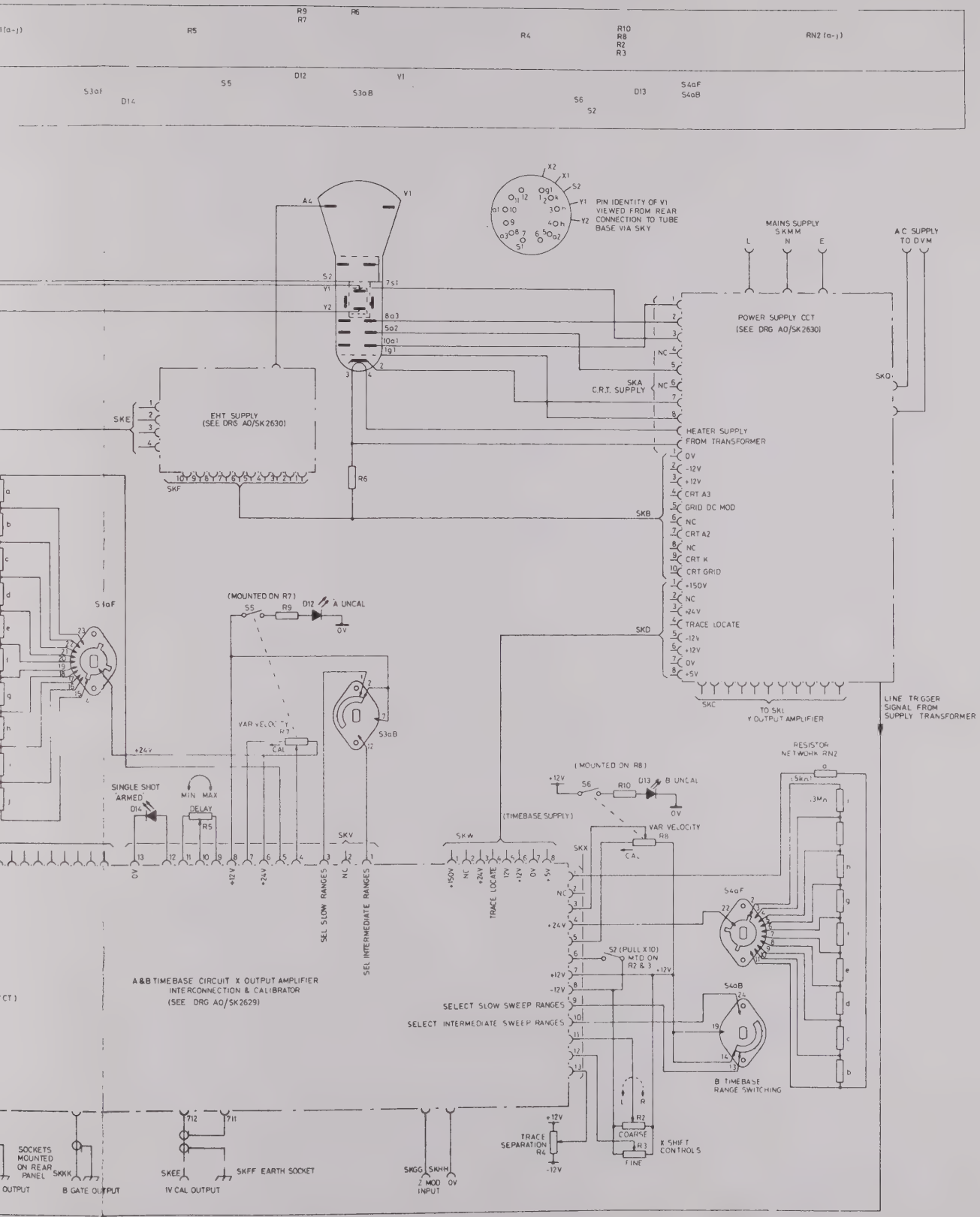


Fig. 12 Interconnection Diagram

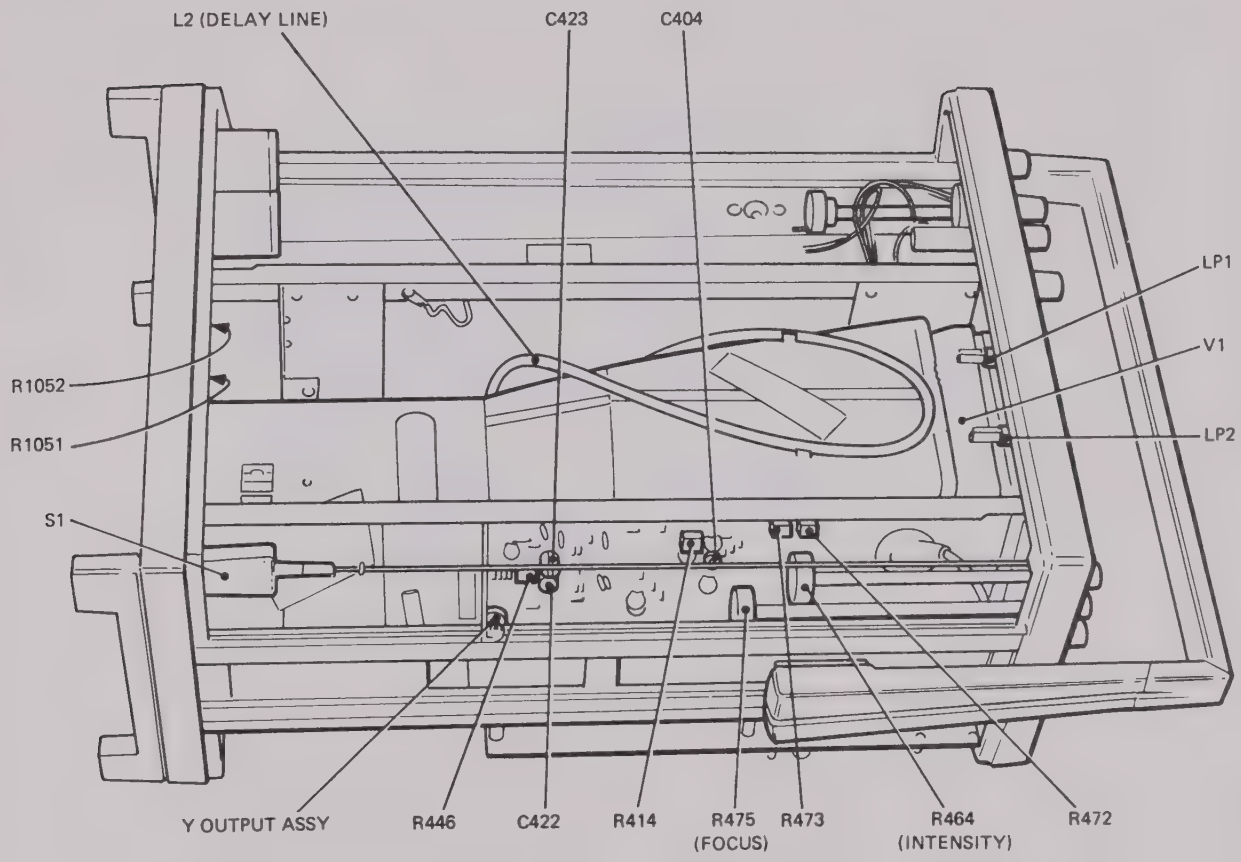


Fig. 13 Component Location Top Left View

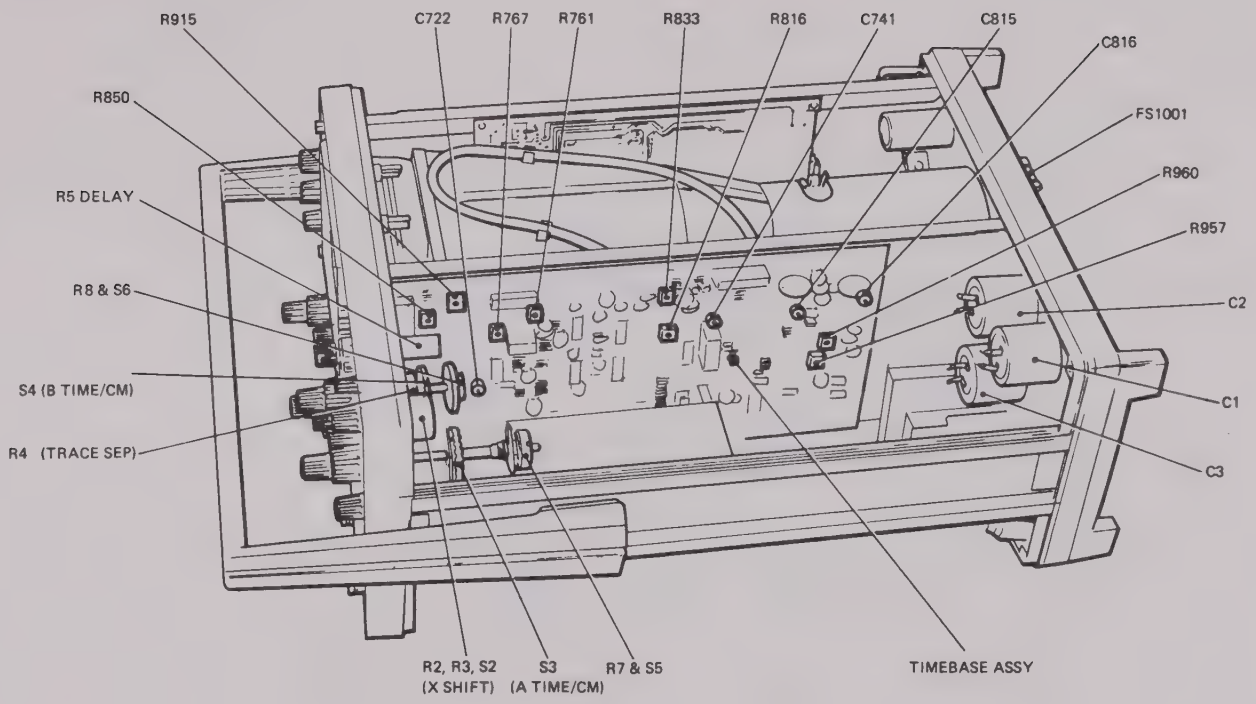


Fig. 14 Component Location Top Right View

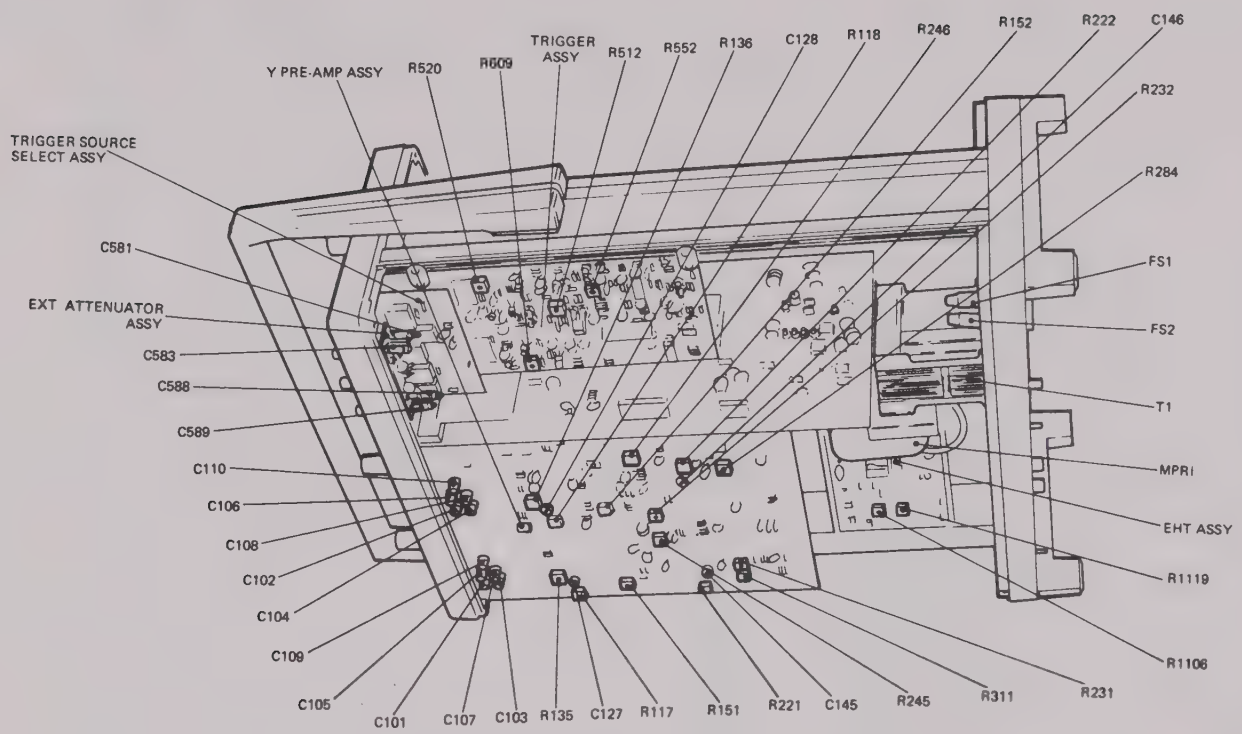
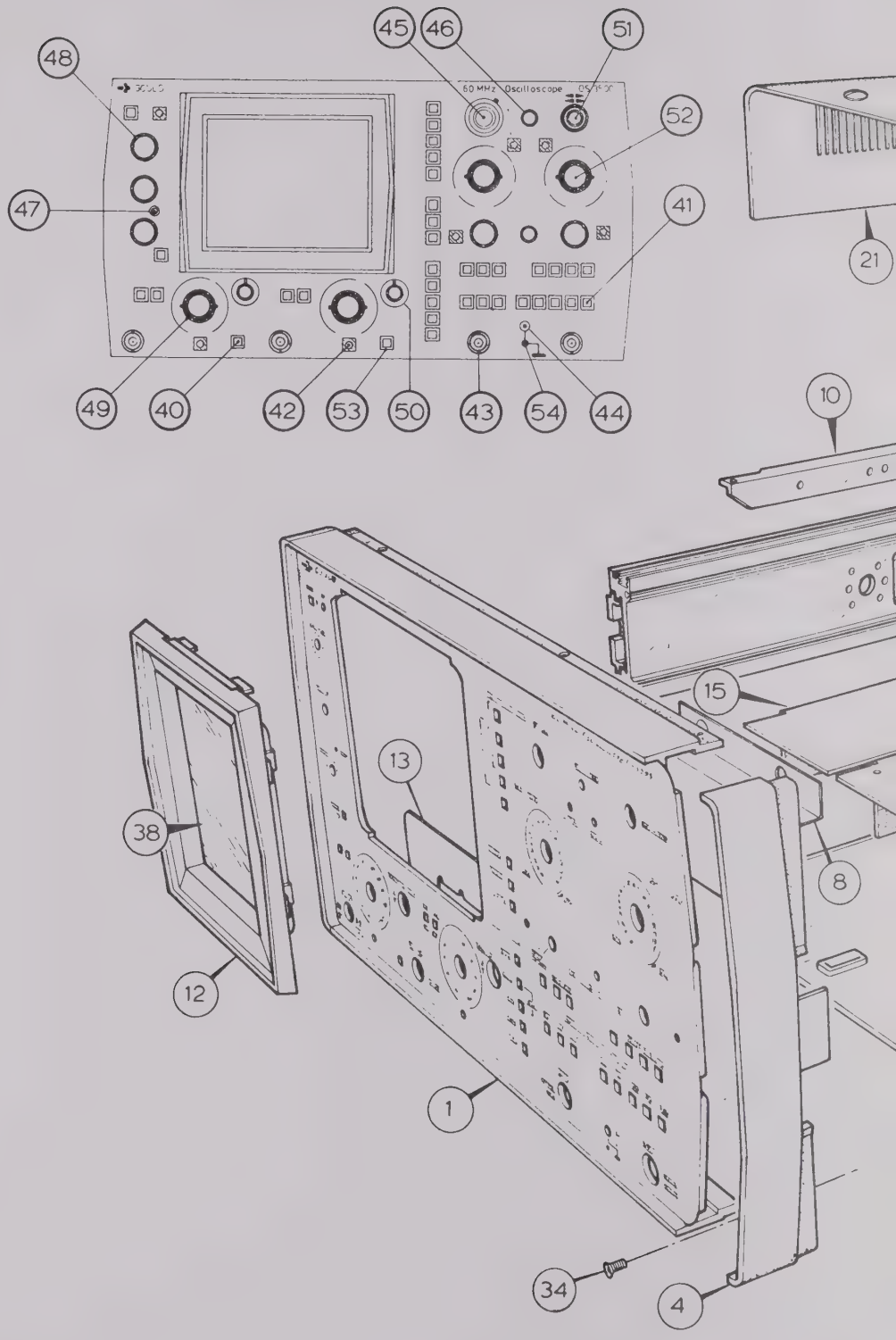


Fig. 15 Component Location Bottom View

OS3500 MECHANICAL PARTS LIST

ITEM No.	PART No.	DESCRIPTION
1	41746	Panel Front Composite
2	40674	Panel Rear
3	42898	Side Support Bar
4	39096	Corner Frame
5	40809	Bracket Support E.H.T. C.R.T.
6	39101	Foot – Rear Support Moulding
7	40805	Handle Assy.
8	40806	Bracket Pot. Mounting
9	40770	Heatsink
10	42355	Bracket P.C.B. Support
11	40829	Bracket P.C.B. Support
12	39100	Bezel Moulding
13	40807	Panel Attenuator
14	43104	Screen Atten. CH2 (Track)
15	43103	Screen Atten. CH1 (Track)
16	41822	Screen (Timebase/C.R.T.)
17	39915	Trim Side Front
18	39916	Trim Side Rear
19	40844	Cover Rear
20	40813	Cover Bottom
21	40812	Cover Top
22	40641	Foot Bottom Cover
23	37864	Latch
24	37915	'0' Ring
25	39097	Block Indexing
26	40677	Spacer to Bracket Assy.
27	40676	Spacer to Bracket Assy.
28	38006	Fuse Holder
29	33685 or 34790	Fuse "
30	29206	Spring
31	32626	Circlip
32	42296	M3 Spacer – Threaded & Tapped
33	33124	M3 Spacer. 10 Long
34	33077	M4 x 12 Screw Cs/Hd.
35	33068	M3 x 6 Cs/Hd. Pos. Screw
36	41764	M4 x 10 Hex Hd. St. Cad. Plate
37	33037	M3 x 6 Pan Hd. Screw
38	40814	Filter Blue (Pt. No. 41381 Filter Amber)
39		
40	40836	Knob P/B Light Brown
41	38407	Knob P/B Dark Brown
42	39884	L.E.D.
43	1222	B.N.C. Socket
44	24159	Insert Feed Thro
45	36851	Dial Counting Knob
46	40408	Knob R2–234
47	40635	M4 ∅ Bush
48	40923	Knob R2–354
49	40410	Knob (Wing) R4–454
50	41812	Nut Cover D/P W7–219
51	40925	Knob R2–124
52	40922	Knob R2–324
53	43256	Bezel – Pushbutton
54	40833	Terminal 4mm Earth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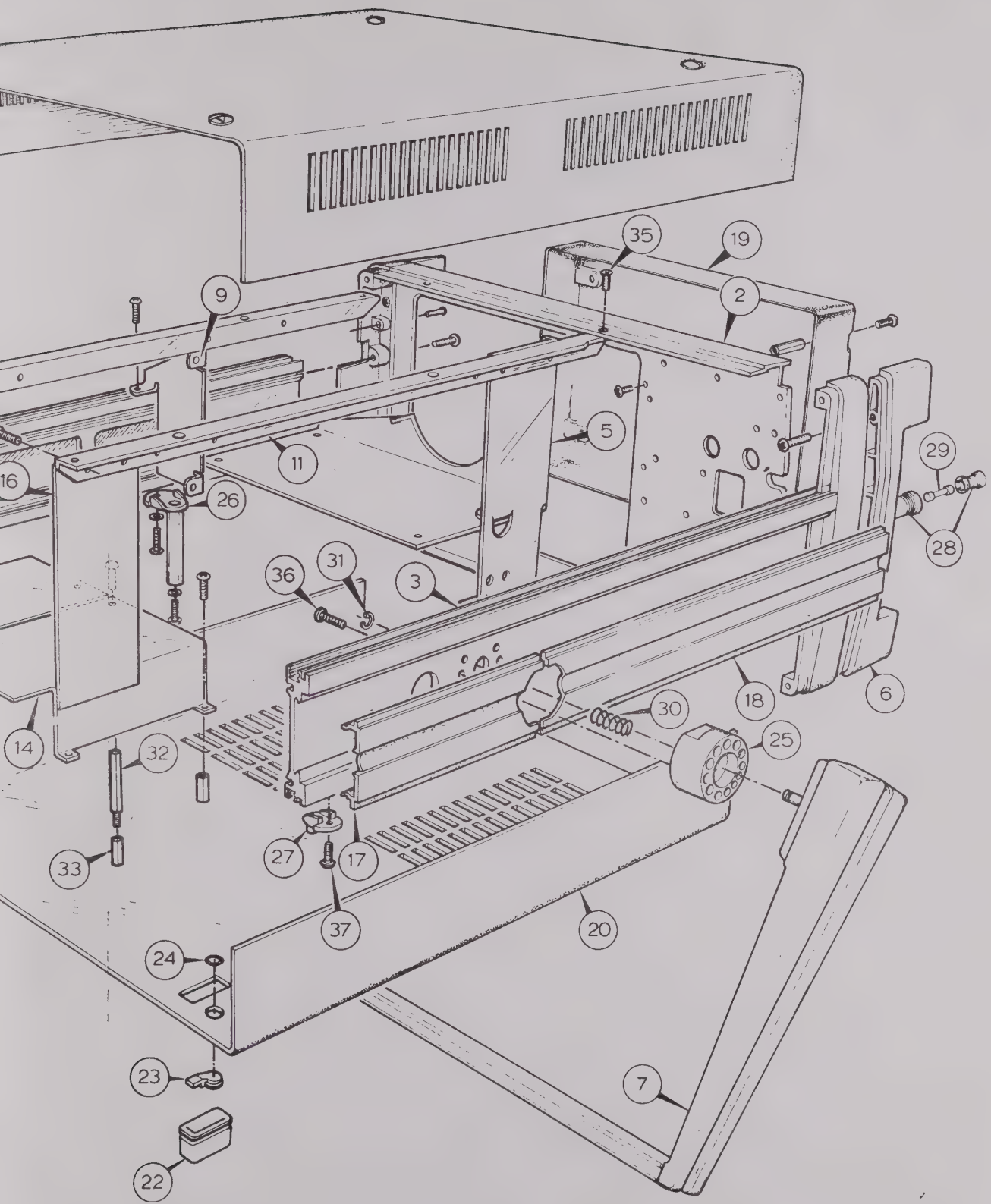

Fig. 16 Mechanical Assembly

SECTION 7

WARRANTY AND SERVICE FACILITIES

Gould Oscilloscopes are warranted for a period of two years from date of shipment to original purchaser. They are warranted to conform to the applicable published specifications in effect at the time of shipment, and to be free from any defects in material or workmanship.

LIABILITY OF THE GOULD INSTRUMENTS DIVISION UNDER SUCH WARRANTY IS LIMITED TO SERVICING OR REPLACING DURING THE WARRANTY PERIOD AT THEIR OPTION, ANY DEFECTIVE PARTS EXCEPT COVERS, PROBES OR FUSES AND DOES NOT INCLUDE CALIBRATION AND MINOR MAINTENANCE AS OUTLINED IN OPERATING MANUALS. IN NO EVENT SHALL THE GOULD INSTRUMENTS DIVISION BE LIABLE FOR COLLATERAL OR CONSEQUENTIAL DAMAGES.

Units are to be returned transportation prepaid by the buyer. The Gould Instruments Division will have the right of final determination of the cause and existence of a defect under this warranty. This warranty shall not apply to any products which have been subjected to misuse, improper installation, repair, alteration, neglect, accident, inundation, fire or operation outside their published maximum ratings.

PACKING INFORMATION

If the unit is to be returned for service, it must be adequately packed as follows:

a) Seal the unit in an oversize plastic bag.

b) Pack the bagged unit into a heavy duty cardboard box. The box must have a minimum of 2 inches of cushioning on all six sides, so that the unit fits snugly.

c) Any accessories or instruction manuals must be sealed into a separate plastic bag and packed with a minimum of 2 inches of cushioning between the instrument and the accessories.

d) Before sealing the box with packing tape, ensure that an official packing note is inserted, giving full details of sender's name, address and telephone number, instrument type number and serial number, plus an indication of the reason for return, and/or fault conditions, if applicable.

e) Properly label and address the outside of the box.

f) Notify Gould in advance of shipment and ship prepaid by United Parcel Service or equivalent.

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129 Middlesex Turnpike
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